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Low Voltage High Accurate Current Mode Analog Multiplier

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Abstract: The Low voltage high accurate current mode analog multiplier is a basic building block in analog signal processing. This proposed circuit is a four quadrant multiplier, designed using squarer circuit. The squarer circuit is designed based on the translinear loop principle. The major advantages of proposed design are low voltage (VDD=1V), high accurate, high bandwidth (122MHZ), less area, and small linearity error. The linearity error is obtained as 0.5%. The simulations of circuit are done in the pyxis schematic editor using Mentor graphics tool with 0.18µm standard CMOS technology.

Keywords: squarer circuit, translinear principle, current mode operation, cascade current mirrors, square difference identity.

1. INTRODUCTION

Signal processing circuits are very widely using in many applications such as in telecommunications, medical equipments, disk drivers and other applications. Even the popular Digital systems also requires analog to digital conversion at the front of the circuit and digital to analog conversion at its end of the device, the analog computation and signal processing makes it simpler and faster. Analog signal processing represents the signals as physical quantities like e.g. charge, current, voltage or frequency. These signals are continuous in value and continuous in time. Multiplication and division of analog signals are difficult operations in analog signal processing.

In Analog signal processing, analog multipliers are used in many applications such as frequency translation, waveform generator, analog modulation, automatic gain controller, squaring and square rooting, RMS to dc conversion, neural networks, VLSI adaptive filters or measuring equipment and curve fitting generators.The analog multiplier is used as basic building block in analog signal processing .In Analog signal processing multiplication operation is somehow difficult, so the analog multipliers are mainly concern about accuracy, speed performance, good linearity errors and circuit hardware which leads to easy of operation in any analog signal processing. Two supply voltages VDD and VSS are used in [1] one is at supply another is at ground node to reduce linearity errors but the power consumption is high. In [2] to reduce power consumption subthreshold region CMOS transistors are designed. In [3] Floating gate MOS transistors are used to design a good analog multiplier. In [4] multiplier circuit used some techniques to reduce power consumption with CMOS transistors leads to circuit complexity. To reduce miss matching effect and linearity errors [5] improved accuracy current mode

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multiplier is designed with NMOS translinear loop. For low voltage high linearity [6] presents a analog multiplier which is good in linearity with the high circuit complexity. With 3.3V a four quadrant multiplier is designed [7] using cascade current mirrors.

In this proposed design the optimized analog multiplier circuit is designed with very small linearity errors and high bandwidth with supply voltage as 1V.

2. THEORETICAL ANALYSIS

The proposed and existing analog multiplier circuits are designed using translinear principle. The stack based translinear loop used in both existing and proposed circuits contains even number of MOS transistors have same Vgs value. By applying squaring characteristics to the translinear equation gives internal node currents ID1, ID2 in existing circuits and I01,I02 in proposed circuit.

2(a) Squaring circuit

The drain source current Ids of an MOS transistor operated in saturation region is given by

IDS =0.5 μ COx W/L (Vgs-Vt) 2 (1)

The below Fig:1 shows the squaring circuit and the transistors M1 M2 M3 and M4 are in translinear loop. Using translinear principle the loop equation of M1 M2 M3 and M4 is given by

2 Vgs Id1 = Vgs Id3 + Vgs Id4 (2)

Applying squaring characteristics to equation

$2\sqrt{ID} = \sqrt{[ID3+ (ID4)]}$ (3)

Using KCL at nodes M3 and M4 then

ID3 =Io + IIN

ID4 =Io - IIN (4)

Substituting equation 4 and 5 in equation 2 gives

Iout = IIN2/4IB +IB (5)

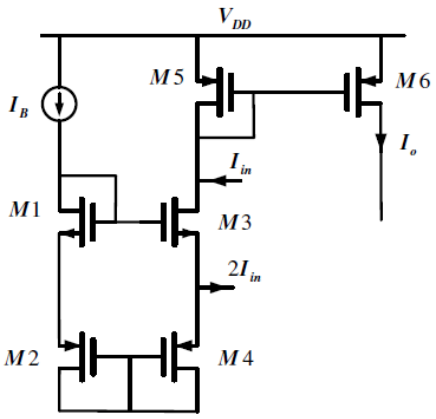

Fig1: squaring circuit

2(b) Existing first implemented analog multiplier and divider circuit

The Fig: 2 show first implementation of multplier/ divider circuit. This consists of a Translinear loop connected with current mirrors to get inputs to it.

The Translinear loops are indicated with curved braces (M1, M2, M3, M4 and M1, M2, M6, M7) and the inputs I1, I0 are given through the current mirrors.

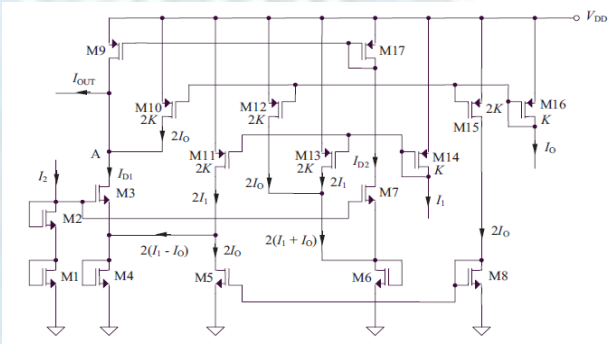

Fig2: First implemented analog multiplier/divider circuit

The current mirrors are used to reduce the mismatching effect and which reduces the linearity errors and improves the speed of the operation of the circuit. By applying Translinear principle to the above Translinear loop the resulting equation is

2Vgs (I2) = Vgs (ID1) + Vgs [ID1+2(I1-I0)] (6)

2Vgs (I2) = Vgs(ID2)+Vgs[ID2+2(I1+I0)] (7)

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Next step is to apply squaring characteristics of MOS transistors operates in saturation region then obtained equation as

$2\sqrt{I2} = \sqrt{(ID2)} + \sqrt{[ID2+2(I1+I0)]}$ (8)

$2\sqrt{I2} = \sqrt{(ID1)} + \sqrt{[ID1+2(I1-I0)]}$ (9)

By doing mathematical analysis for equations8and 9 the internal current values ID1, ID2 were obtained as

$$I_{D1,2} = I_2 - (I_1 \mp I_0) + \frac{(I_1 \mp I_0)^2}{4I_2}. \quad (10)$$

The impedance node 'A' which is presented at the multiplier/divider circuit gives the nodal (KCL) equation as

Iout = ID2 - ID1 +2I0 (11)

By substituting ID1, ID2 (eqn10) values in eqn11 then we will get final multiplier/divider output current as

$$\text{Iout} = \frac{\text{ID1 ID2}}{I_0} \quad (12)$$

2(c) Second implemented analog multiplier and divider circuit

Fig3 shows the second implementation of multiplier/divider circuit, has similar block diagram as first multiplier circuit with more number of transistors. The equations of the Translinear loop contain M1, M2, M4, M5 and M8, M10, M11, M12 gate-source voltages.

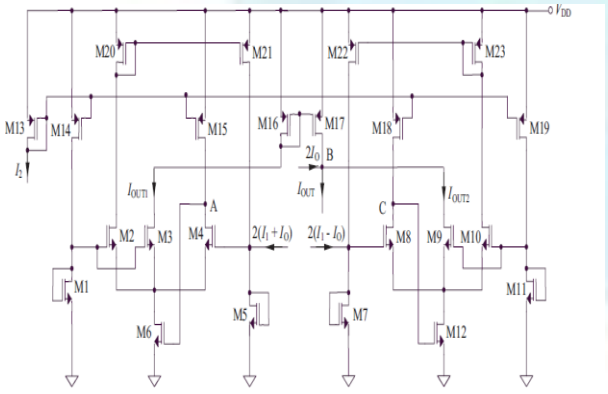

Fig3: The second implementation of multiplier/divider circuit.

The internal currents Iout1 and Iout2 are derived same as first implemented multiplier. And they can be obtained as

$$I_{OUT1} = I_2 - \frac{2(I_1 + I_0)}{2} + \frac{4(I_1 + I_0)^2}{16I_2}. \quad (13)$$

Similarly the Iout2 equation is obtained by replacing the I1+I0 with I1-I0. By applying nodal at node C the output current can be obtained as

Iout = Iout1 – Iout2 +2I0 (14)

By substituting equations 13 in Eqn14 gives the overall output current.

$$\text{Iout} = \frac{\text{ID1 ID2}}{I_0} \quad (15)$$

2(d) Proposed current mode Analog multiplier

Fig4 shows the new squarer proposed to overcome the difficulties imposed by [7] the squarer MOS translinear law in saturation region, for M1 to M4 transistors we have

(KNMOS= KPMOS, VTH,N= VTH,P) (16)

By cascading squaring circuit which is in Fig1 then the four quadrant analog multiplier circuit will obtained. The Four quadrant current mode analog multiplier is shown in Fig:4

By using mathematical equation i.e., square difference identity:

(X+Y)2 - (X-Y)2 = 4XY (17)

Using dual translinear loops and giving input currents Ix+ Iy and Ix- Iy the Iout is obtained as

Iout = Io1- Io2 (18)

By substituting Ix+ Iy in equation6 Io1 is obtained as

I01= (Ix+ Iy) 2/4IB + IB (19)

By substituting Ix- Iy in equation6 Io2 is obtained as

. I02 = (Ix- Iy) 2/4IB + IB

(20)

Substituting these two equations (19,20) in Eqn 18 gives the overall output current Iout is

$$\text{Iout} = \frac{\text{Ix Iy}}{I_0} \quad (21)$$

3. SIMULATION RESULTS

3(a) Simulation results for existing circuits

The Fig:2 represents schematic diagram of first multiplier/divider circuit .The circuit operation depends on Translinear loop and inputs of multiplier (I1,I0)is given through the current mirrors .the transistors which are mirrored with input terminal having 2K of aspect ratio .The theoretical output of

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the multiplier/divider circuit obtained by using eqn12 .There are three inputs need to give to the circuit for first simulation by varying the input I1 current from 0 to 10 μA, I0 fixed at 40μA and the input I2 current has a parametric variation: 1) 10 μA;2) 20 μA; 3) 30 μA; and 4) 40 μA. These simulations are shown in Fig5. And by exchange the values of inputs three inputs need to give to the circuit by varying the input I2 current from 0 to 10 μA, I0 fixed at 10μA and the input I1 current has a parametric variation: 1) 10 μA; 2) 20 μA; 3) 30 μA; and 4) 40 μA. These simulations are shown in Fig6.

Similar to that of first assumption inputs, the second implemented circuit simulations are made by the theoretical output of the multiplier/divider circuit obtained by using eqn12 .second circuit simulations are shown in Fig7, Fig8.The obtained simulation for multiplier/divider circuit in Mentor graphic, ELDO simulator.

3(b) Simulations for proposed analog multiplier/divider circuit

The current mode analog multiplier circuit is shown in Fig:2 inputs current is ranges between +/-10μA.Ix=10μA, and Iy is varies from -10 to 10μA and IB is constant input current at 10μA. Obtained output current values are shown in Fig9: and Fig:10

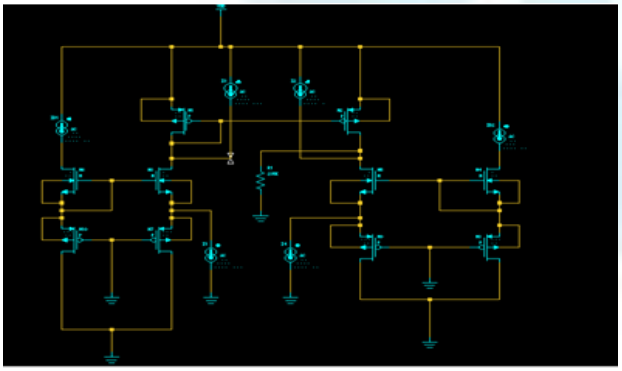
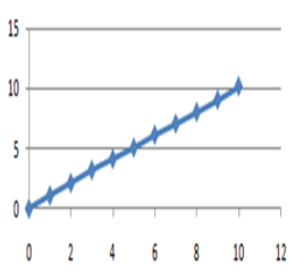
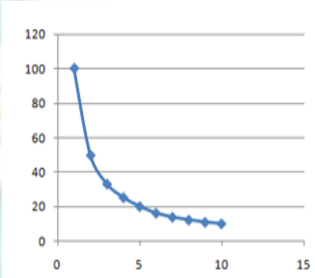


Fig4: New current mode analog multiplier



I1 in uA	theoretical values in uA	practical values in uA
0	0	0
1	1	1.106
2	2	2.14
3	3	3.2185
4	4	4.1491
5	5	5.0887
6	6	6.1546
7	7	7.079
8	8	8.048
9	9	9.0633
10	10	10.186

Fig5: simulations for I2=40 μA, I0 =40 μA, and I1 = 0 to 10 μA



I2 in uA	theoretical values in uA	practical values in uA
0	0	0
1	100	100.476
2	50	49.951
3	33.3	33.3
4	25	25.43
5	20	20.23
6	16.6	16.38
7	14.285	14.05
8	12.5	12.416
9	11.11	11.122
10	10	10.23

Fig6: simulations for I2=10 μA, I0 =10 μA, and I2 = 0 to 10 μA

I_1 in μA	Theoretical values	Practical values
0	0	0
1	2μA	2.0165μA
2	4μA	4.0121μA
3	6μA	6.0127μA
4	8μA	8.0159μA
5	10μA	10.0185μA
6	12μA	12.0481μA
7	14μA	14.0509μA
8	16μA	16.1098μA
9	18μA	18.1239μA
10	20μA	20.264μA

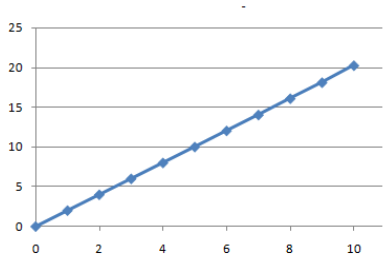


Fig7: simulations for I2=20 μA, I0 =40 μA, and I1 = 0 to 10 μA

I_2 in μA	Theoretical values	Practical values
0	0	0
1	200 μA	200.0095μA
2	100μA	100.125μA
3	66.66μA	66.6746 μA
4	50μA	50.016 μA
5	40μA	40.020μA
6	33.33μA	33.3665μA
7	28.571μA	28.610μA
8	25μA	25.0565μA
9	22.22μA	22.2865 μA
10	20μA	20.075μA

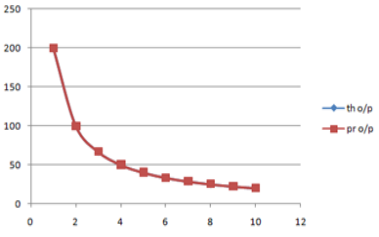


Fig8: simulations for I2=20 μA, I0 =10 μA, and I2 = 0 to 10 μA

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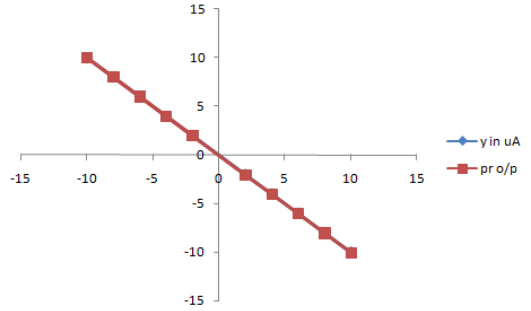

Fig9: multiplier/divider output for Iy=-10uA

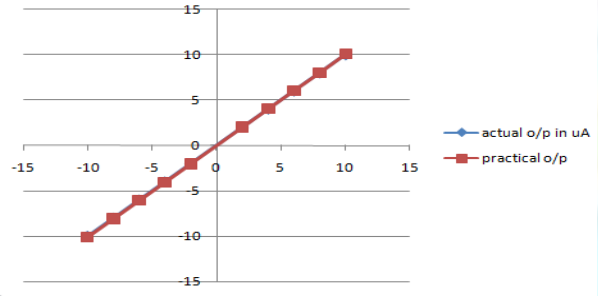

Fig10: multiplier/divider output for Ix=10uA

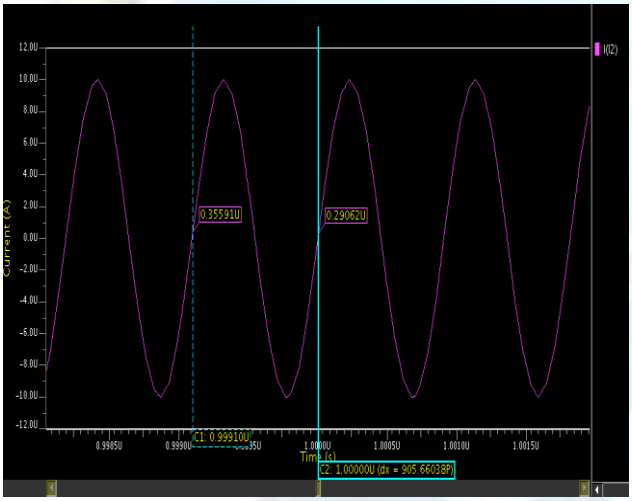

Fig11(a): Input current (Ix+Iy) waveform

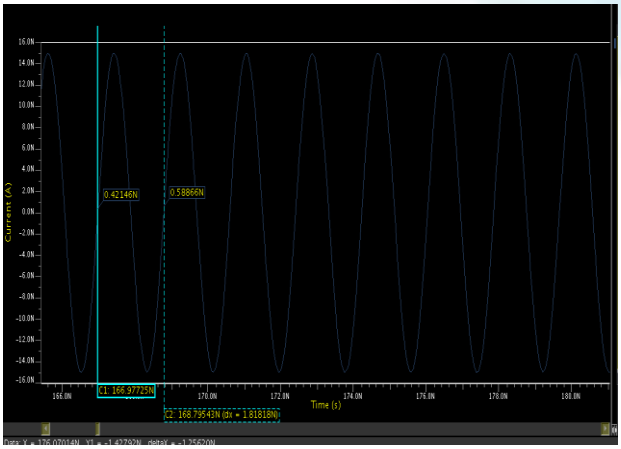

Fig11 (b): Input current (IB) waveform

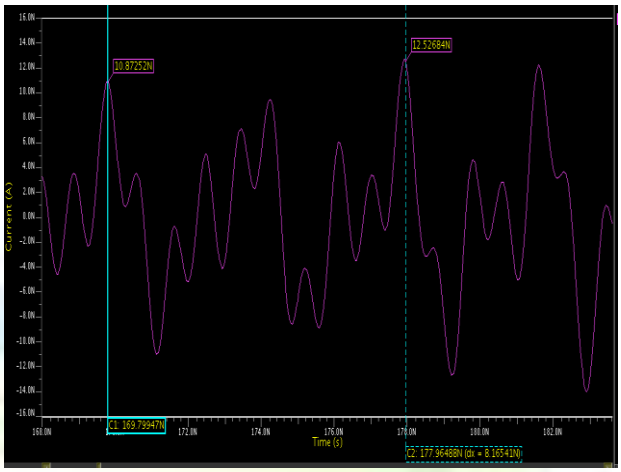

Fig11 (c): output waveform

Fig11: simulation results for linearity error

The linearity error is defined as the difference between absolute value and obtained value.

Linearity error % = (Iout-Iout|)*100

Linearity error simulations for first and second circuits were shown in Fig12.the linearity error is 0.75% and 0.9% respectively.

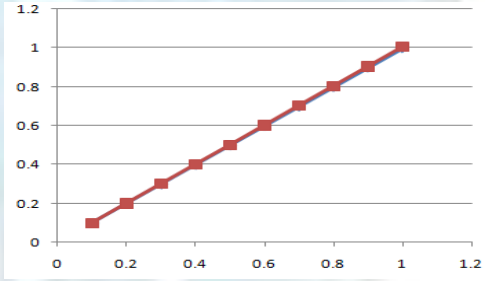

Fig12(a) simulation for linearity error of 1st implemented circuit

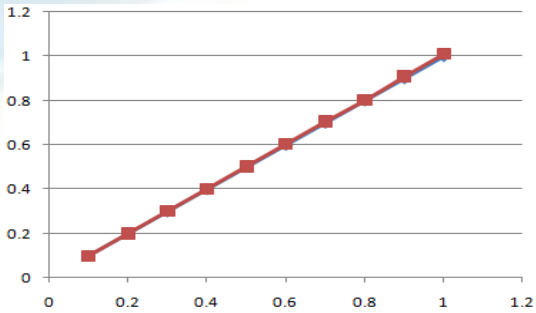

Fig12 (b) simulation for linearity error of 2nd implemented circuit

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And the simulations of proposed analog multiplier circuit linearity errors are shown in Fig11 (c).the linearity error is obtained as 0.5% ,bandwidth of the circuit is 122MHZ with (Ix= 10 sin (2π×1e6 t) μA and Iy= 5 sin (2π×1e5 t) μA) the all simulations are run using Mentor Graphics with 0.18μm standard CMOS technology.

4. COMPARISONS BETWEEN PREVIOUS DESIGNS TO PROPOSED DESIGN

Existing implementations of two original analog multiplier circuits are good in one quadrant multiplication, but the proposed work is can do four quadrant multiplication operations with good linearity. And bandwidth of the circuit is very high when compared to previous works .Comparisons are shown in Table1

Table1: comparison results

Reference number	[1]	[5] Existing	[6]	[7]	This work
Technology(μm)	0.5	0.18	0.18	0.35	0.18
V_{DD} in (V)	+/- 1.5	1.2	1	3.3	1
Linearity error %	1.2	0.75	0.6	1.1	0.5
Bandwidth in MHz	19	79.6	59.7	41.8	122
quadrants	Four	One	one	four	four

5. CONCLUSION

This proposed design of current mode analog multiplier is designed with high linearity, high bandwidth less area, and supply voltage. The current-mode operation of the proposed computational structures further increases the circuit's accuracy. And this circuit can deals with positive as well as negative input currents and gives corresponding outputs. So it can also know as four quadrant analog multiplier/divider circuit.

The proposed structures have extremely low linearity errors (0.5%). The minimal value for the supply voltage of 1V was obtained for implementing the proposed computational structures in 0.18-μm CMOS technology and was correlated with the model parameters associated with this technology. It is possible to implement the proposed circuits in processes of 0.13 nm, having much lower values of the threshold voltages and, in consequence, allowing a much smaller value of the minimal supply voltage (even less than 1 V). Another important factor that contributes to the small value of the minimal supply voltage is represented by the proposed architecture of the multiplier/divider circuit, compatible with low-voltage operation (avoiding any cascode stages and having a current-mode operation). The circuit bandwidth is 122MHz respectively, while their power consumption is low.

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