



Analog and Digital PLL with Single Ended Ring VCO for “Full Swing Symmetrical Even Phase Outputs”

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Abstract— The most versatile application of a phase locked loop (PLL) is clock generation and clock recovery in microprocessors, networking, wired and wireless communication system and frequency synthesizers. Voltage controlled oscillators (VCO) are the important and crucial building block in the PLL. This paper proposes a “Single Ended Type Ring VCO with a New Delay Cell” for Full Swing Symmetrical Even Phase outputs. To meet the requirements of high-quality performance in portable device systems at low cost, a ring VCO structures of numerous differential delay cells have been commonly implemented in recently developed VCO monolithic integrated chips (ICs). However, compared with ring VCOs of single-ended delay cells, implementing ring VCOs of differential delay cells typically require a larger area, greater power consumption and a tail current circuit. Therefore, determining a method for designing a “Single Ended Ring-type VCO” with a wide tuning range, a small layout area ((without a tail current circuit) and high Signal to Noise Ratio (SNR) is crucial. Therefore, the designed Ring VCO is placed in PLL and simulates the miscellaneous blocks of phase locked loop (PLL). In addition that the proposed VCO with a new delay cell achieved (16.6-33) MHz wide tuning range with full swing symmetrical even phase outputs, which yielded -174.28dbc/Hz phase noise at 1MHz, occupied small layout area with only 5 *transistors* delay cell and consumed less power approximated to 0.48Megawatts operated at only 1.2V supply voltage in TSMC 180nm deep submicron technology.

Index Terms—Analog and Digital Phase Locked Loop, Band Switch Function, Full Swing, Low Power VLSI circuits, Ring Oscillator, Signal to Noise Ratio, Single Ended Delay cell, Symmetrical Even Phase, Tuning Range, Voltage Controlled Oscillator.

I. INTRODUCTION

A phase locked loop is a circuit which is widely used in modern integrated circuits design. It is a feedback system that compares the output phase /frequency with the input phase/frequency. PLLs are utilized for frequency synthesis, carrier synchronization, carrier recovery, frequency division, frequency multiplication, and frequency demodulation [1]. Voltage controlled oscillator is the heart of the PLL. It is an oscillator, varies the output frequency in according to the input voltage. The overall performance of the PLL is depends on the performance of VCO. To meet the requirements of portability, electronic products increasingly use low-voltage, high signal-to-noise ratio (SNR) monolithic integrated chips. Therefore, an effective design for a low-voltage full-swing on-chip VCO is needed.

On-chip CMOS VCO technology is typically implemented in ring oscillators and inductor-capacitor (LC) oscillators. Compared with LC structures, ring structures provide a wider tuning range, smaller layout Area, lower dissipated power, more output phases and less design complexity [11], [12]. To achieve high-quality performance in portable device systems at low cost and with a simple design, ring VCO structures of numerous differential delay cells have been commonly implemented in recently developed VCO integrated circuits [3], [10], [13], [14]. However, compared with ring VCOs of single-ended delay cells, implementing ring VCOs of differential delay cells typically require a larger area, greater power consumption, and a tail current circuit. Therefore, determining a method for designing an even-phase ring-type VCO with a wide tuning range, a simple design with small

layout area (without a tail current circuit) and high SNR is crucial.

Another major concern in VCO design is the variation in the output phase and frequency as a result of noise on the control line. For a given noise amplitude, the noise in the output frequency is proportional to the VCO gain (KVCO). Thus, the noise on the control line can be reduced by minimizing the KVCO. But, there is a tradeoff between phase noise and tuning range. To overcome it, VCO requires a "band switch function". It reduces the noise in the control line as well as improves the tuning range [15]. Accordingly, full-swing single-ended delay cell with band switch function is a good architecture for designing VCOs.

The ring VCO proposed in this paper uses a novel single-ended delay cell and is designed to achieve the requirement of a low-supply voltage, high SNR, linear frequency-voltage characteristics, Full swing symmetrical even-phase outputs [16]–[18], and a band switch function. The performance of the four-phase output of the VCO is especially critical.

A challenging work is to design a low phase noise, less power consumption ring oscillator using a charge pump (CP) phase locked loop in CMOS technology. Because it has been designed for high bandwidth. A design presented here is to improve the overall characteristics of PLL. The another component of the PLL is the Phase Frequency Detector (PFD) which has been designed to improve the speed by minimizing the dead zone. The main part of this PLL is the VCO, which has been designed to get superior phase noise.

II. LITERATURE REVIEW

Two widely used VCO types are LC tank based and CMOS ring circuits. The LC tank circuit is the combination of inductor and capacitor. It occupies large layout area and consumes more power. CMOS ring based oscillators have advantages because easy to control output frequency and no requirement of on chip inductor. CMOS based ring oscillators gives wide tuning range and easy to integrate. Due to their integrate nature ring oscillator have becomes one of the most important

building block in many digital and communication system. The ring architecture can implement with two different structures. Single ended and differential ended delay cells. A ring VCO for even phase outputs with differential structure requires "tail current circuit" which consumes more power than single ended structure. The single ended structure is more advantageous than differential interns of power and area.

III. SYSTEM OVERVIEW

Phase locked loops (PLLs) generate well timed on chip locks for various applications such as clock and data recovery, microprocessor clock generation and frequency synthesizer. The basic concept of phase locking has remained the same since its invention in the 1930s [1]. However, design and implementation of PLLs continues to be challenging in design requirements of a PLL such as clock timing uncertainty, power consumption and area become more stringent. This section briefly describes about the architecture of the PLL. The basic form of PLL consists of five main blocks:

1. Phase frequency detector (PFD).
2. Charge pumps (CP).
3. Low pass filter (LPF).
4. Voltage controlled oscillator (VCO) and
5. Frequency divider

To synchronize the frequency, various types of PLLs are being used in the application of wireless communication. In addition with the VCO, the PFD compares feedback signal with input signal and generates the error signal. The CP circuit along with LPF is used to minimize the disturbances at the input of VCO which achieves a sharper and smooth signal at the VCO output.

VCO is heart of the PLL. The overall performance of the PLL is depends on the performance of the VCO. In this design the VCO implemented with a "Single Ended Ring type oscillator with a new Delay Cell". Conventional single-ended ring oscillators consist of a series of inverting amplifiers placed in a feedback loop and are composed of an odd number of inverters. For this reason, the conventional single-ended ring oscillator cannot provide symmetrical even-phase outputs. However, many practical applications require an even-phase output. Conventional

single-ended ring VCOs are rarely used in integrated chips because of their poor performance in symmetrical even-phase outputs. Most of the VCOs designed with differential ring oscillators. Nevertheless, the single-ended ring VCO is clearly superior in terms of power consumption and SNR.

Ring oscillators also require sufficient loop gain to initiate oscillation. Loop gain is usually insufficient in the two-stage ring oscillator. Therefore, four-phase output ring oscillators with differential delay cells are usually implemented using four-stage architectures that have high-power consumption [2], [14].

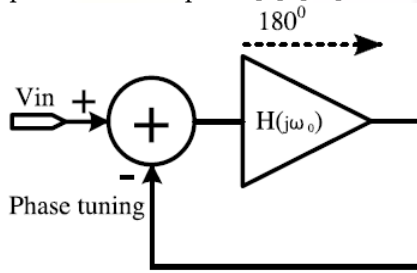


Fig. 1. Oscillatory feedback system.

Compared with conventional differential delay cell topologies, the inverter base ring VCO with the current reuse technique provides a higher amplifier transconductance (g_m) of the VCO without increasing power dissipation. Therefore, the inverter base ring VCO reduces power consumption. Moreover, the inverter base ring VCO technique provides full-swing output and improves the SNR of the VCO. The VCO proposed in this paper is an inverter base ring VCO that provides an even-phase output. Fig. 1 shows the proposed oscillatory feedback system, and Fig. 2 shows the proposed single-ended delay cell circuit. To meet the Barkhausen criterion Fig. 1 shows that the proposed ring oscillator has a frequency-dependent phase shift of 180° (dashed by the arrow) and a dc phase shift of 180° . Therefore, the phase tuning device Mn1 (in Fig. 2) must provide a dc phase shift of 180° . That is, node Vin and node phase tuning must have a 180° phase difference. Moreover, the operating frequency of the proposed VCO can be adjusted by changing ω_0 , which is the 3-dB bandwidth of the delay cell.

A. Single ended delay cell for even phase outputs

The single-ended delay cell ring VCOs were used for implementing a full swing symmetrical even-phase output. The attractive feature of the VCO includes improvement in power dissipation,

tuning range and linear frequency-voltage characteristics. Fig. 3 shows an input simplified equivalent circuit of the proposed single-ended delay cell circuit shown in Fig. 2. The 3-dB bandwidth of each stage is derived as follows:

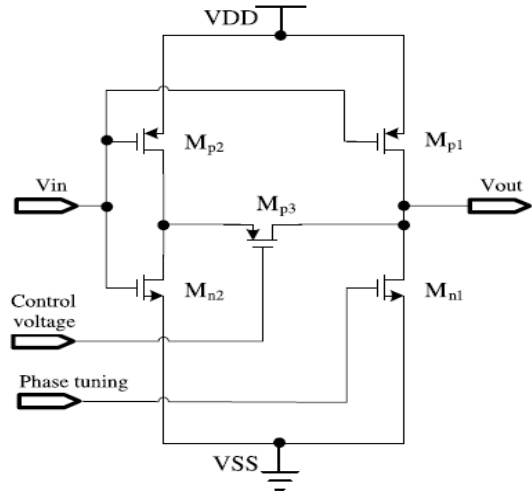


Fig. 2. Single-ended delay cell circuit.

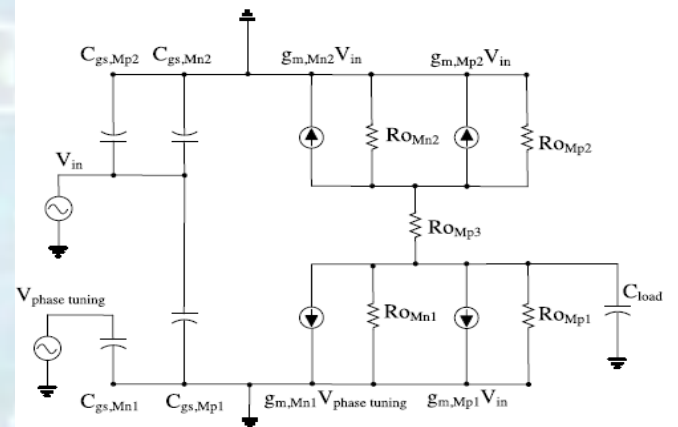


Fig. 3. Small signal simplified equivalent circuit of the single-ended delay cell in Fig. 2.

The 3-db bandwidth of each stage is derived as following

$$\omega_0 = \frac{1}{\{(RoMn1 // RoMp1) // [(RoMn2 // RoMp2) + RoMp3]\} Cload}$$

where $RoMn1$, $RoMp1$, $RoMn2$, $RoMp2$, and $RoMp3$ are the ON-resistances of Mn1, Mp1, Mn2, Mp2, and Mp3, respectively; and $gm\ Mn1$, $gm\ Mp1$, $gm\ Mn2$, and $gm\ Mp2$ are the transistor transconductances of Mn1, Mp1, Mn2, and Mp2, respectively. The $Cload$ is the input equivalent capacitance of the next stage. According to these concepts, the control voltage can be changed by adjusting the ON-resistance of transistor (Mp3) to achieve a 3-dB bandwidth tuning technique. Thus, the output frequency of the VCO can be changed

by varying the control voltage.

IV. VCO ARCHITECTURE

The proposed ring VCO, which employs four stages, is feasible.

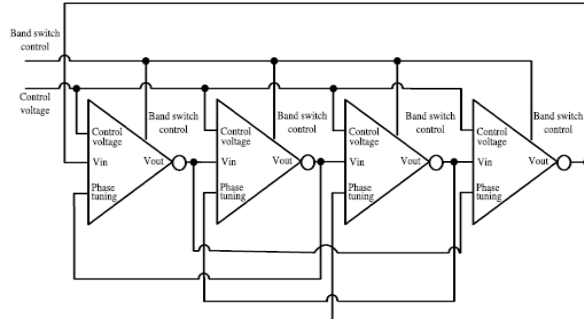


Fig. 4. Proposed four-stage ring VCO based on single-ended delay cells.

The total number of proposed delay cells in the loop must be even so that the proposed VCO can provide even-phase outputs (the output-phases are determined by the stages of VCO). The performance of symmetrical four-phase ring-type VCO was improved using the proposed single-ended delay cell, as shown in Fig. 6. In addition, the proposed architecture can be validated by this experiment. The waveforms of proposed VCO shown in fig. 7.

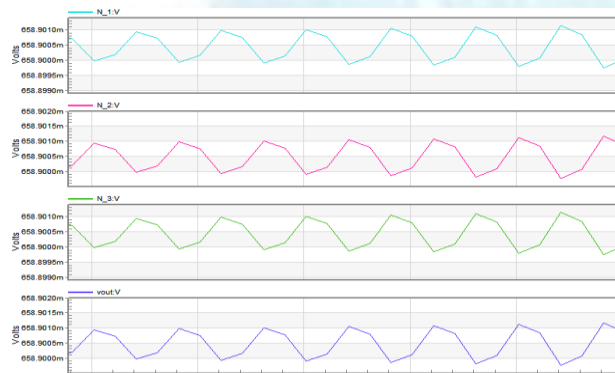


Fig. 5. Output waveform of the proposed four-phase VCO

The VCO was designed using a Taiwan Semiconductor Manufacturing Company 0.18- μm CMOS process with a 1.2 V supply voltage. The power consumed by the VCO is 0.48mW and the tuning range is 16.6MHz to 33MHz. The phase noise is -174.76dbc/Hz.

V. PHASE FREQUENCY DETECTOR

A phase frequency detector (PFD, is a device which compares the phase of two input signals and provides a signal in the form of phase error. It has two inputs which correspond to two different input signals, usually one from a current starved voltage controlled oscillator and other is a reference source. It has two outputs which instruct subsequent circuitry on how to adjust to lock onto the phase. The fig 6 shows phase frequency detector.

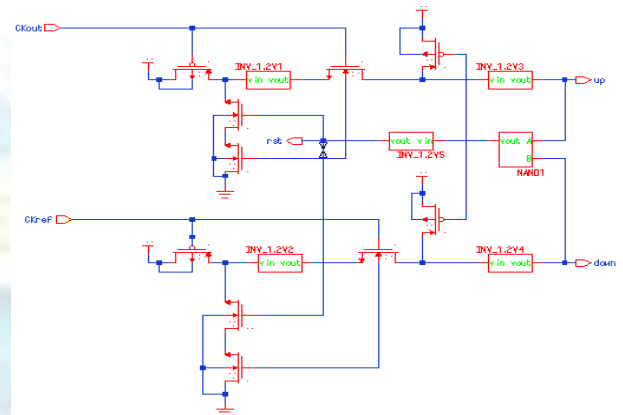


Fig. 6. The phase frequency detector

If there is a phase difference between the two signals, it will generate "UP" or "DOWN" Signals. When the reference clock rising edge leads the feedback input clock rising edge "UP" signal goes high while keeping "DOWN" signal low. On the other hand if the feedback input clock rising edge leads the reference clock rising edge "DOWN" signal goes high and "UP" signal goes low. Fast phase and frequency acquisition phase frequency detectors are generally preferred over traditional Phase frequency detectors. The output waveforms o phase frequency detector is as shown in fig-7.

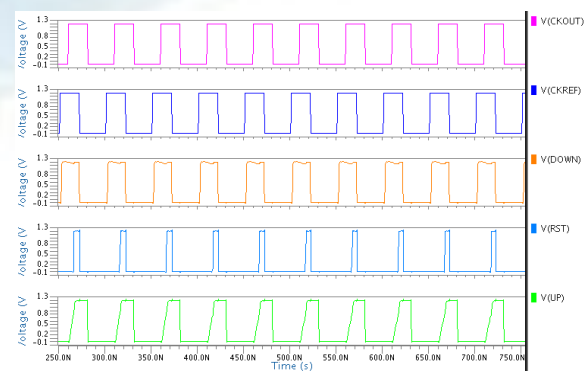


Fig. 7. Output waveform of the Phase Frequency Detector

VI. CHARGE PUMP

A charge pump circuit is used to convert the digital signal from the phase frequency detector to analog signal, the output of which is used to control the frequency of the voltage control oscillator. The output of the PFD should be combined into a single output to drive the loop filter. In Figure (5) charge pump, two NMOS and two PMOS are connected serially. The uppermost PMOS and lowermost NMOS are considered as the current source and the other PMOS and NMOS in the middle are connected to the "Up" and "Down" of the output of PFD, respectively When the PFD "Up" signal goes high, the PMOS will turn on. This will connect the current source to the loop filter. It is in the similar way when the PFD "Down" signal goes high. The charge pump along with PFD is as shown in fig.8.

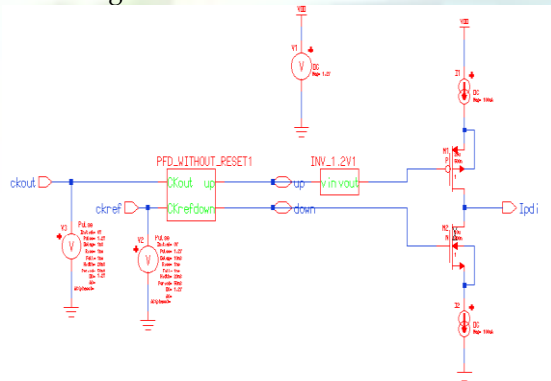


Fig. 8. Charge pump with PFD

VII. LOOP FILTER

The function of the loop filter is to convert the output signal of phase frequency detector to control voltage and also to filter out any high frequency noise introduced by the PFD. The loop filter shown in Figure (9) used with this type of PFD is a simple RC low-pass filter. Since the output of the PFD is oscillating, the output of the loop filter will show a ripple as well, even when the loop is locked. This modulates the clock frequency, an unwanted characteristic of a DPLL using PFD. A ripple on the output of the loop filter with a frequency equal to the clock frequency will modulate the control voltage of the VCO. A high speed low power consumption positive edge triggered Delayed (D) flip-flop was designed for increasing the speed of counter in Phase locked loop, using 180 nm CMOS technology.

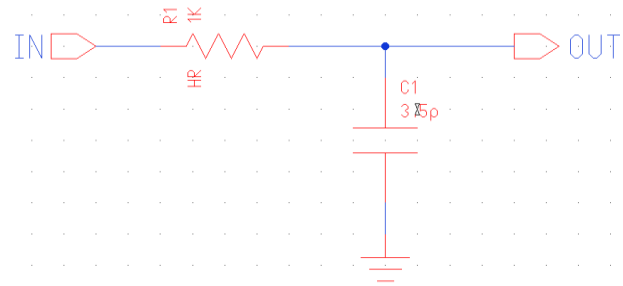


Fig.9. Low pass filter

VIII. FREQUENCY DIVIDER

Frequency divider divides the VCO frequency to generate a frequency which is comparable with reference frequency. Here we used divide by 2 network, we can vary the divider network for synthesis of different frequencies. It divide the clock signal of VCO and generate clock as shown in figure (10), and then applied to phase frequency detector which compare it with input data.

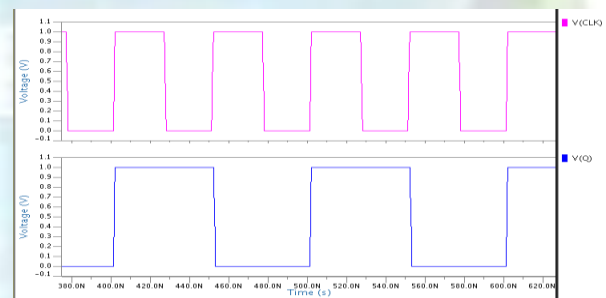


Fig.10. wave forms of frequency divider

IX. CONCLUSION

The application of portable devices is popular and crucial, especially in communication, medical care and consumer electronic products. VCOs are the heart of every wired and wireless communication systems, including phase lock loop, clock data recovery, serial link radio, digital millimeter radar, CPU, delay locked loop, and microprocessor-based systems. However, proposed VCO with a new delay cell achieved (16.6-33) MHz wide tuning range with full swing symmetrical even phase outputs, which yielded -174.28dbc/Hz phase noise at 1MHz, occupied small layout area with only 5 transistor delay cell and consumed less power approximated to 0.48Megawatts operated at only 1.2V supply voltage in TSMC 180nm deep submicron technology. Simulated by Mentor Graphics pyxis

schematic Editor.

Parameters	Proposed design	Current starved oscillator[4]
Operating frequency	16.6-33MHz	1-25MHz
Supply voltage	1.2V	2V
Process	0.18um	0.35um
Power dissipation	0.48mW	11.93mW
Phase noise	-174db/Hz	No
Full swing	Yes	No
Even phase outputs	Yes	No

Table1: Performance comparisons of Proposed design with current starved inverter as shown below.

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