

# Application of Facts Technology to Power System Protection in the Nigerian 330kv Network Using Genetic Algorithm

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**Abstract:** - This paper focused on Fault current limitation in the Nigerian 330kV Power Network. The strategy adopted is the use of a genetic algorithm to optimize the proportional integral (PI) control parameters of the Unified Power Flow Controllers (UPFC). Also, the SIMULINK model of the Nigerian 330kV system was developed. Then, the result from the simulation carried out proved the versatility of UPFC on fault current limitation in the power system when the PI parameter is optimized using genetic algorithm. This indicates that the UPFC achieved an effective average of 59.23% fault current limitation. The result is shown to have high impact for protection of critical assets within the power system such as circuit breakers. At a fault impedance of 0.0001Ω, the UPFC provided a 45.81% protection margin for the type of high voltage circuit breakers used in the 330kV system.

**Keywords:** Fault Current Limitation, Genetic Algorithm, Protection, Unified Power Flow Controller and Proportional Integral.

## 1. Introduction

In the present power system, the increasing rate of energy demand leads to the increase in the addition of more generation and transmission systems to the national grid. As unwelcome consequences of the above fact, fault currents are increasing day-to-day [1]. Many utilities all over the world are experiencing the problem of astonishing short circuit current (fault current) levels [1]. Faults on power systems are inevitable due to external or internal causes. Lightning may strike the overhead lines causing insulation damage. Incidences of downed or crossed power lines also cause faults. During a fault, an excessive current

called fault current flows very high and may exceed ten times the rated current of an equipment [2]. These large currents can damage or degrade circuit breakers and other expensive transmission and distribution components [3].

It is well established that the fault current levels in a network increases proportionally with the addition of lines and new generation. This is found in the Nigerian 330kV system, especially the addition of transmission and generation components to the system as a result of the National Integrated Power project (NIPP). This implies that the short-circuit current rating (i.e the fault current withstand) of existing

transmission assets on the Nigerian 330kV system will be exceeded. Increasing the rate of fault current levels on power systems can cause undesired consequences which may be summarized as follows.

- Equipment is exposed to unacceptable thermal stresses;
- Equipment is exposed to unacceptable electro-dynamic forces;
- Short-circuit breaking capability of high voltage circuit breakers are typically limited to 80kA [4];
- In order to prevent equipment damage, faster circuit breakers are required. This requirement faces both technical and economical restrictions.
- Step and touch voltages are also increased as a result of increasing short circuit levels. This will cause safety problems to the personnel;
- Switching over voltage transients will become more severe, due to significant short circuit currents.

These problems put more pressure on power system protection equipment and their configuration. Furthermore the fault clearing time of conventional protection system (Relay/Circuit breaker) is not instantaneous, for it depends on the operating time settings of over current relay and the circuit breakers tripping time. Hence a system that can swing faster into action to limit the destructive effects of the fault current is necessary.

Due to the above-mentioned problems, the subject of fault current level reduction has gained a considerable attention in recent years among electric utilities [5]. The idea behind this line of protection research is to reduce the stress within the network or limit the stress over certain assets. However, a number of fault current limitation techniques have been introduced in several publications and they include superconducting fault current limiter [6][7], HVDC links [8] and current limiting reactor [9] [10]. The superconducting fault current limiters use superconducting material such as NDT and MgB<sub>2</sub> to transfer from superconducting state to the normal state, if exposed to high current levels. Although this limiter seems to be an ideal fault current limiter, it is still too expensive, especially due to the cost of its complicated cryogenic system. HVDC links are used to diminish inter-area short-circuit current. However, it is reported that this method is not economically justified. Among

the excessive fault current limiting methods indicated, the current limiting reactor is argued to be the most practical approach. However it is reported [11] that current reactor may degrade both voltage stability and transient stability of the power system.

Consequently a more versatile protection technique becomes necessary. Such technique should possess almost instantaneous response to fault and have dynamic and enhanced power control capability. Genetic algorithm for the optimization of proportional integral of the UPFC fits into this requirement. This technology eliminates the use of bulky equipment that shows the operation of circuit breakers, and it can use highly sophisticated semiconductor devices such as Thyristors, GTOs or IGBTs [11][12][13].

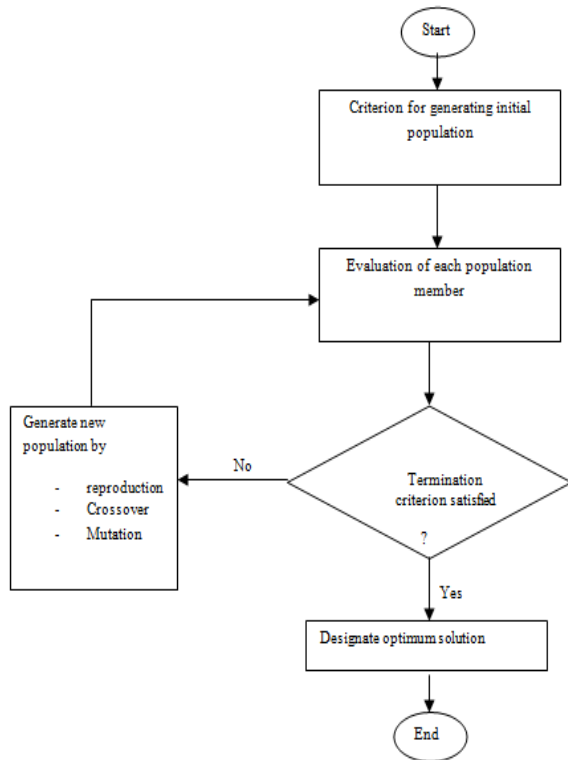
The speed, the power transfer and control capabilities of FACTS can be applied to enhance the protection of the Nigerian 330kV transmission system from destructive over currents. Considering the shortcomings of the fault current limitation techniques as briefly pointed out earlier in this paper, the problem confronting this work is the application of genetic algorithm in the optimization of proportional integral of unified power flow controller (UPFC) to improve the protection of the Nigerian 330kV power system by effectively limiting destructive fault currents.

The main objective of this work is to use genetic algorithm to optimize the proportional integral of unified power flow controller (UPFC) for the protection of the Nigerian 330kV network without further upgrade or replacement of existing equipment. This paper is significant because it will reduce the operating and managerial costs in terms of protection of utility equipment in the Nigerian 330kV power system. Therefore, both the network operators and customers will benefit immensely as it will enhance economic benefits and reliability in power system. The paper is a practical approach of power transfer and control capability of proportional integral for the protection of 330kV system from excessive fault current.

## II. Genetic Algorithm

The Genetic Algorithm, GA, according to Rao in [14] is a powerful optimization searching technique based on the principles of natural genetics and natural selection. A flow of the general scheme of the

implementation of the GA is shown in figure 1.



**Figure 1:** General flow chart of the Genetic Algorithm.[15]

In the GA, normally the design variables, corresponding to the genomes in the natural genetic, are represented as binary strings and they are concatenated to form an individual, corresponding in turn to a chromosome in natural genetics. Other representation can be used. However, a binary representation is more adequate if an implementation in a digital system has to be carried out. There are two basic parameters of Genetic Algorithm (GA): crossover probability and mutation probability.

**Crossover probability** is how often the crossover is performed. If there is no crossover, offspring is exact copy of parents. If there is a crossover, offspring is made from parts of parents chromosome. If crossover probability is 100%, then all offspring is made by crossover. If it is 0%, whole new generation is made from exact copies of chromosomes from old population (but this does not mean that the new generation is the same).

Crossover is made in hope that new chromosome will have good parts of old chromosomes and may be the new chromosomes will be better. However it is reported in the literature [16] that it is good to leave some parts of population survive to next generation.

**Mutation probability** is how often the parts of chromosomes are mutated. If there is no mutation, offspring is taken after crossover (or copy) without any change. If mutation is performed, parts of chromosomes are changed. If mutation probability is 100%, whole chromosomes are changed, if it is 0%, nothing is changed. Mutation is made to prevent falling of GA into local extreme, but it should not occur very often, because the GA will in fact change to random search [17].

**Population size** is how many chromosomes are in a population (in the generation). If there are too few chromosomes, GA have a few possibilities to perform crossover and only a small part of search space is explored [18]. On the other hand, if there are too many chromosomes, GA shows down. Research shows that after some limit (which depends mainly on encoding and the problem) it is not useful to increase population size, because it does not make solving the problem faster [19].

### III. Model Design and Analysis

The proportional integral (PI) controller is a vital component of the UPFC control structure. The control design proposed here is based on the optimization of the PI control parameter ( $K_p$ ,  $K_i$ ) using genetic algorithm. The technique is to use the proportional integral (PI) controllers in the UPFC controllers (shunt and series controllers) to dynamically adjust the phase angle between the FACTS devices voltage source converters (VSCs) and the power system bus voltage in order to adaptively generate or absorb energy at the connection point during a fault transient. To achieve this, the strategy is to use the combination of the Phase Locked Loop (PLL) and the UPFC shunt and series PI controllers to generate pulse sequence that controls the magnetic coupling of the energy interchange between the FACTS devices and the power system.

Analysis of the fault current limiting effect of the UPFC is developed to explain the impact of limiting fault current at the fault point. The analysis given in this section shows the dynamics of the FACTS device series injected voltage in limiting the impact of the fault, having protecting key assets on the power transmission system. Actually what is happening between the FACTS devices and the power system is energy interchange. If this interchange between the power electronics and the power system

can be adaptively controlled, the system can be made to react in the event of fault current hence limiting the fault current by quickly absorbing energy at the connection point.

Hence, the strategy adopted here is to use the PLL and the UPFC PI controllers (with the PI controller parameter optimized using Genetic algorithm) to generate pulse sequence that controls the magnetic coupling of the energy interchange between the FACTS devices and the power system. Most of the injected voltage which is quadrature with the size current, emulates an inductive or a capacitive reactance in series with the transmission line. This emulated variable reactively inserted by the injected voltage source, influences the electric power flow through the transmission line.

## IV. Analysis of the Fault Current Limitation of UPFC device

The idea behind the destructive fault-current limitation concept is to minimize the voltage at the fault point through the action of the injected series voltage,  $V$ . This, in fact, is an extension of the Thevenin's pre-fault voltage concept at the fault point. Based on this, Figure 2 is used to present the analysis. For the case of a three-phase fault occurring at bus 3 (Figure 2), it can be seen the contribution of the two independent loops L (left) and R (right) to the fault point. In fact, the series voltage will reduce the current contribution from the left AC system ( $E_i$ ).

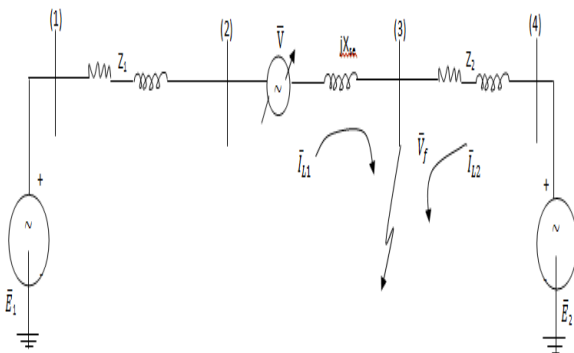


Figure 2. Series VSC Converter seen as a fundamental Frequency for fault.

This reduction will be more effective when the UPFC injects positive sequence voltages in opposition to the

left equivalent source, which can be estimated in each operative condition. If it is intended to minimize the total current at the fault point, the series voltage injected must be in opposition to the pre-fault voltage at the fault point. As the voltage along the line has a smooth behavior, it is not difficult to set values to cover some other cases of fault along the compensated line.

Initially, it will be defined the left and right equivalent impedances, from the fault point up to each AC source, as  $Z_L$  and  $Z_R$ , respectively. For a phase-to-ground fault, which is the case more likely to occur, to minimize the current contributions to the fault, a more careful analysis must be performed. Such an analysis can be done through phase or sequence components.

Thus, regarding the fault point considered in Figure 2 which can be located at any point along the line  $Z_2$ , and with the term  $X_{se}$  included within the equivalent impedance  $Z_L$  (left side), it can be established that

$$[E_1^1] = [E_1] + [V] \text{ --- (1)}$$

Under the absence of the fault, the line current in the system will be

$$[I_L] = [Z_L + Z_R]^{-1} [E_1^1 - E_2] \text{ --- (2)}$$

The pre-fault voltage at bus 3 can be expressed as

$$[V_3] = [E_2] + [Z_R][I_L] \text{ --- (3)}$$

Substituting (2) into (3) and calling  $M$  the matrix that represent the voltage divider, yields:

$$[V_3] = ([I] - [M])[E_2] + [M][E_1] + [M][V] \text{ --- (4)}$$

Where  $[I]$  represents the identity matrix. Also

$$[M] = [Z_R][Z_L + Z_R]^{-1} \text{ --- (5)}$$

In order to simplify (4), the first two terms (i.e those affected by  $E_1$ ,  $E_2$  without the effect of  $V$ ) will be named as  $V_{uf}$  (uncompensated fault voltage), whereas the last term will be designated as  $V_{sc}$  (series compensated voltage at the fault point F). Thus, the compensated fault voltage ( $V_f$ ) in (6), former  $V_3$ , becomes:

$$[V_f] = [V_{uf}] + [M][V] \text{ --- (6)}$$

To minimize  $V_f$ , the compensation term  $[M][V]$  has to be in opposition to  $V_{uf}$ , with the series voltage ( $V$ ) being inserted at its maximum possible magnitude during fault period. The contribution of the coupling effect of unaffected phases to the fault currents limitation has to be considered. The inductive effect of the unaffected phases is analyzed. Hence, if the product of the resulting impedance matrices in (5) were renamed as that shown in (7), where to simplify the analysis transposed lines are considered.

$$[M] = \begin{bmatrix} \alpha & \beta & \beta \\ \beta & \alpha & \beta \\ \beta & \beta & \alpha \end{bmatrix} \dots (7)$$

Factors  $\alpha$ ,  $\beta$  are dependent on the equivalent impedance  $Z_L$  and  $Z_R$  and on the zero and positive sequence values which define the coupling effect between phases. The substitution of (7) into (6), yields:

$$\begin{bmatrix} \bar{V}_{fa} \\ \bar{V}_{fb} \\ \bar{V}_{fc} \end{bmatrix} = \begin{bmatrix} \bar{V}_{ufa} \\ \bar{V}_{ufb} \\ \bar{V}_{ufc} \end{bmatrix} + \begin{bmatrix} \alpha & \beta & \beta \\ \beta & \alpha & \beta \\ \beta & \beta & \alpha \end{bmatrix} \begin{bmatrix} \bar{V}_a \\ \bar{V}_b \\ \bar{V}_c \end{bmatrix} \dots (8)$$

For instance, the corresponding terms affecting the fault point at phase "a", are:

$$\bar{V}_{fa} = \bar{V}_{ufa} + \alpha \bar{V}_a + \beta(\bar{V}_b + \bar{V}_c) \dots (9)$$

For the case of the system depicted in Figure 2, if  $Z_{L1} = 0.25$ ,  $Z_{L0} = 0.545$ ,  $Z_{R1} = 0.25$ ,  $Z_{R0} = 0.8695$ , then, the value of the factors  $\alpha$  and  $\beta$  computed, will be:  $\alpha = 0.538$  and  $\beta = 0.038$ . Thus, according to (9) two different strategies can be adopted for analyzing the effect of the voltage V (i.e the series voltage).

- (a) Regarding the positive sequence in the three phases ( $\bar{V}_a + \bar{V}_b + \bar{V}_c = 0$ ), then, the voltage V at phase a will be:

$$\bar{V}_{fa} = \bar{V}_{ufa} + (\alpha - \beta)\bar{V}_a \dots (10)$$

In this case, the unaffected phases can introduce a destructive effect on the voltage at the fault point.

- (b) With the introduction of the zero sequence voltage ( $\bar{V}_a = \bar{V}_b = \bar{V}_c$ ) equation (9) becomes:

$$\bar{V}_{fa} = \bar{V}_{ufa} + (\alpha + 2\beta)\bar{V}_a \dots (11)$$

The voltage control is improved compared to the previous positive sequence voltage compensation.

$\bar{I}_1, \bar{I}_2, \bar{I}_0$ : sequence components of the fault current  $\bar{I}_{L1}, \bar{I}_{L2}, \bar{I}_{L0}$ : sequence components of the left-side equivalent contribution.

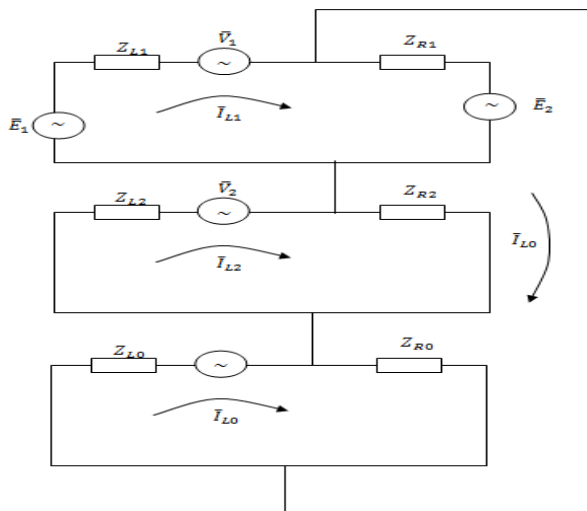


Fig. 3: Phase-to-ground: Equivalent Square Diagram

The loop equation from the diagram shown in figure 3.8 is:

$$\begin{bmatrix} \bar{E}_1 + \bar{V}_1 - \bar{E}_2 \\ V_2 \\ V_0 \\ E_2 \end{bmatrix} = \begin{bmatrix} (Z_{L1} + Z_{R1}) & 0 & 0 & -Z_{R1} \\ 0 & (Z_{L2} + Z_{R2}) & 0 & -Z_{R2} \\ 0 & 0 & (Z_{L0} + Z_{R0}) & -Z_{R0} \\ -Z_{R1} & -Z_{R2} & -Z_{R0} & (Z_{R1} + Z_{R2} + Z_{R0}) \end{bmatrix} \begin{bmatrix} \bar{I}_{L1} \\ \bar{I}_{L2} \\ \bar{I}_{L0} \\ \bar{I}_0 \end{bmatrix} \dots (12)$$

Or in its compact form:

$$[E] = [Z][I] \dots (13)$$

Voltages  $\bar{V}_1, \bar{V}_2$  and  $\bar{V}_0$  are the sequence components of the series voltage injected by the UPFC.

Recalling also that  $[I] = [Y][E]$ ----- (14)

Where:  $[Y] = [Z]^{-1}$ , then the zero sequence fault current can be obtained through (15)

$$\bar{I}_0 = Y_{41}\bar{E}_1 + (Y_{41} - Y_{44})\bar{E}_2 + (Y_{41}\bar{V}_1 + Y_{42}\bar{V}_2 + Y_{43}\bar{V}_0) \dots (15)$$

The first two terms of the second member in (14) represent the fault current without the presence of the series voltages. The remaining terms represent the contribution of the series voltages. Obviously, the fault current can be obtained through:

$$\bar{I}_f = 3\bar{I}_0 \dots (16)$$

Equation (13), is in accordance to the concept of minimizing the pre-fault voltage at the fault point and it shows the most significant effect of applying positive or zero sequence voltage by analyzing admittance matrix terms with positions  $Y_{41}$  or  $Y_{43}$ , similarly to the analysis developed in (10) and (11). The left-side equivalent contribution to the fault current is obtained as follows:

$$\bar{I}_L = (\bar{I}_{L1} + \bar{I}_{L2} + \bar{I}_{L0}) \dots (17)$$

This current is obtained through the addition of the first three rows in (13) in which the equivalent admittance are defined as:

$$Y_j = \sum_{i=1}^3 Y_{ij} \dots (18)$$

Where,  $Y_j$  is composed by the sum of the first three elements of each column.

A similar expression to that shown in (13) can be developed for the left side current contribution ( $\bar{I}_{LC}$ ) to the fault current. That is:

$$\bar{I}_{LC} = \underbrace{Y_1\bar{E}_1 + (Y_1 - Y_4)\bar{E}_2 + Y_1\bar{V}_1 + Y_2\bar{V}_2 + Y_3\bar{V}_0}_{\bar{I}_{LU} \text{ (uncompensated)}} + \underbrace{\bar{I}_{LSC}}_{\text{contribution of V}} \dots (19)$$

Again, the first two terms of the second member in (18) refers to the fault current contribution without the series voltage ( $\bar{I}_{LU}$ ), whereas the remaining terms refer to the series voltage contribution ( $\bar{I}_{LSC}$ ). In order to

minimize the contribution, the total fault current,  $\bar{I}_{LSC}$  must be in opposition to  $\bar{I}_{Lu}$ . The best strategy for applying either the positive or zero sequence voltage from  $\bar{V}$ , for each specific system, must be chosen analyzing the elements  $Y_1$  and  $Y_3$  defined in (17). For example, using the parameters previously given, its respective Y matrix can be obtained:

$$Y = -j \begin{bmatrix} Y_1 & & & \\ 0.0615 & 0.018 & 0.034 & 0.0361 \\ 0.018 & 0.0615 & 0.034 & 0.0361 \\ 0.034 & 0.034 & 0.0875 & 0.0679 \\ 0.0361 & 0.0361 & 0.0679 & 0.0729 \end{bmatrix} \quad \text{--- 20}$$

For this case,  $Y_1 = j0.1135pu$  and  $Y_3 = -j0.1554pu$ , thus, the values computed for the current in (20) result in.

$\bar{I}_{Lu} = 15.46 \angle -95.56^\circ pu$ ,  $\bar{I}_{LSC} = 5.25 \angle 87^\circ pu$ ,  $\bar{I}_{Lu} = 10.22 \angle 96.87^\circ pu$ . For this particular system, the zero sequence application of the series voltage,  $V$ , becomes more effective to reduce the left equivalent contribution to the fault current.

## V. PI Control Parameter Optimization Using Genetic Algorithm

The PI control structure is part of the shunt controller and the series controller blocks. Its parameters  $K_p$  and  $K_i$  determine the effectiveness of its control signal to the switches and the logic block that control the magnetic coupling of energy to the power system feeders.

The setting of these PI parameters constitutes tuning the PI controllers. Instead of tuning these parameters manually genetic algorithm would be very powerful in the optimal tuning of these control parameters. Coding is mapping a parameter to be optimized into one individual from code space to parameter space by some rules.

Because binary system coding is easy for genetic algorithm operation, in this design the PI controller

parameters  $K_p$ ,  $K_i$  are encoded into 5 digit binary system code (and put into one individual). Mapping from binary coding to real number is as shown below

$$x = \text{Min} + \frac{(\text{Max} - \text{Min})}{2^n - 1} \times \text{binary value} \quad \text{--- (21)}$$

Where, Max and Min are upper and lower limits of  $K_p$ ,  $K_i$  respectively, binary value is a binary system value.

Values are randomly assigned for each individual in a specified variable range and convert it into the parameter of the fitness function value i.e  $k_p$ ,  $k_i$  when evaluating the fitness population members.

Initial population is randomly generated, they are converted to bit strings and fitness is assigned. The fitness of the chromosomes are:

$$\text{fitness value} = \frac{1}{\text{performance Index}} \quad \text{--- (22)}$$

The fitness formation is taken as inverse of error. i.e. performance index, because the smaller the value of performance indices of the corresponding chromosomes the fitter the chromosome will be, and vice versa.

This design uses equation (23) as crossover probability method in which crossover probability will diminish with generation increase.

$$P_c = P_{c1} \left(1 - \frac{m}{M}\right) \quad \text{--- (23)}$$

Where  $m$  is evolution generation,  $M$  is the total generation, generally  $P_{c1}$  is 0.6 – 0.8 [52].

Mutation probability used is given by equation (3.43) [52]

$$P_m = P_{m1} \left(1 - \frac{m}{M}\right) \quad \text{--- (24)}$$

Where  $m$  is evolution generation,  $M$  is the total generation, generally  $P_{m1}$  is 0.1 [51].

## VI. Simulation and Result Evaluation

The Nigerian 330kV power system was used to simulate and assess the effectiveness of the proportional integral of the UPFC in limiting fault currents in the Network. The system is modeled in MATLAB and SIMULINK model of the 330kV system is given in Figure 4.

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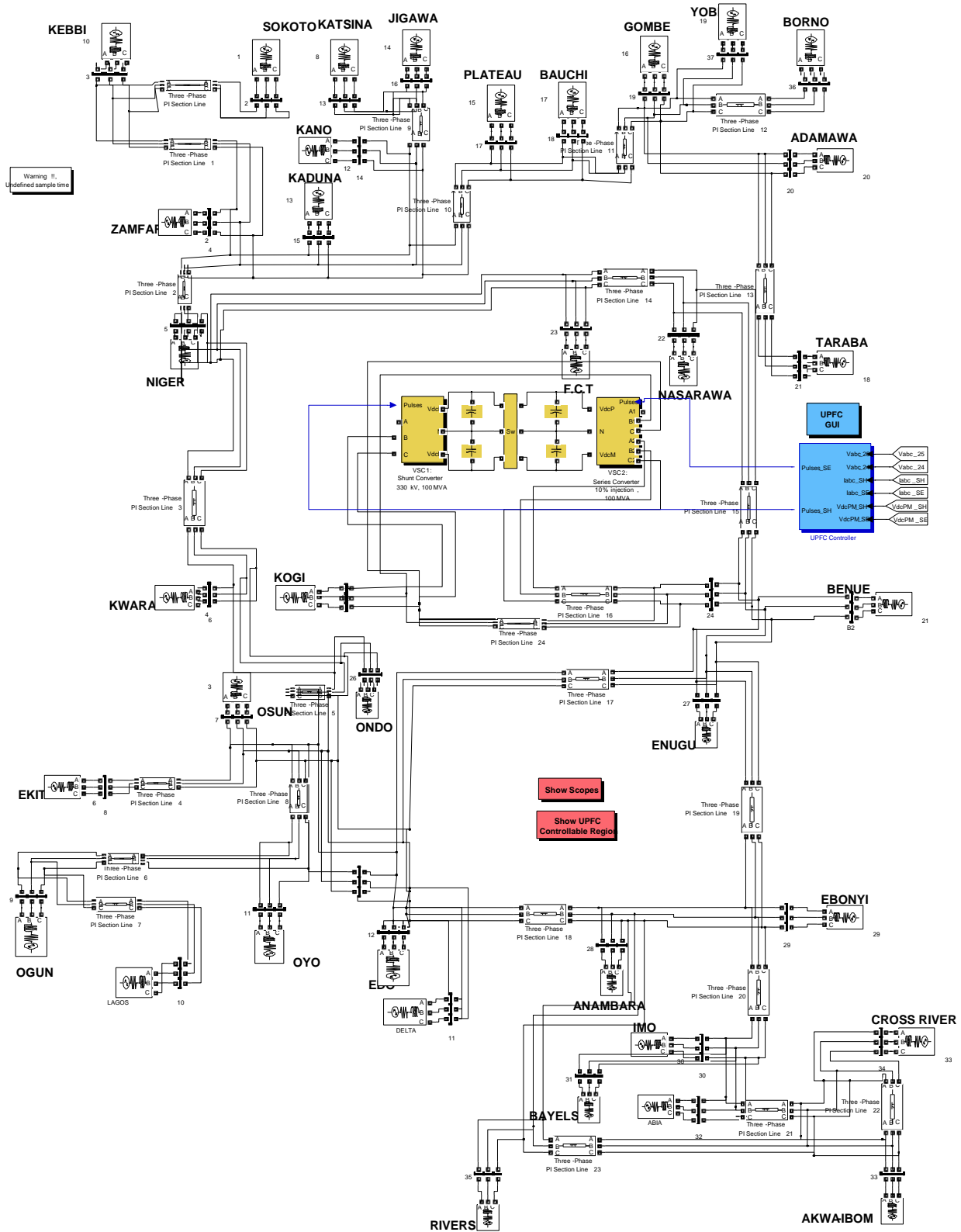


Figure 4: Simulink Model Of The Nigerian 330Kv Power System With Upfc Integrated For Protective Fault Current Limitation

The further detail on the control components of PLL and PI parameter are shown in fig 5. The PI controllers as indicated in Figure 5 is vital to the control of the

pulse sequences required to control energy injection or absorption to the feeders.

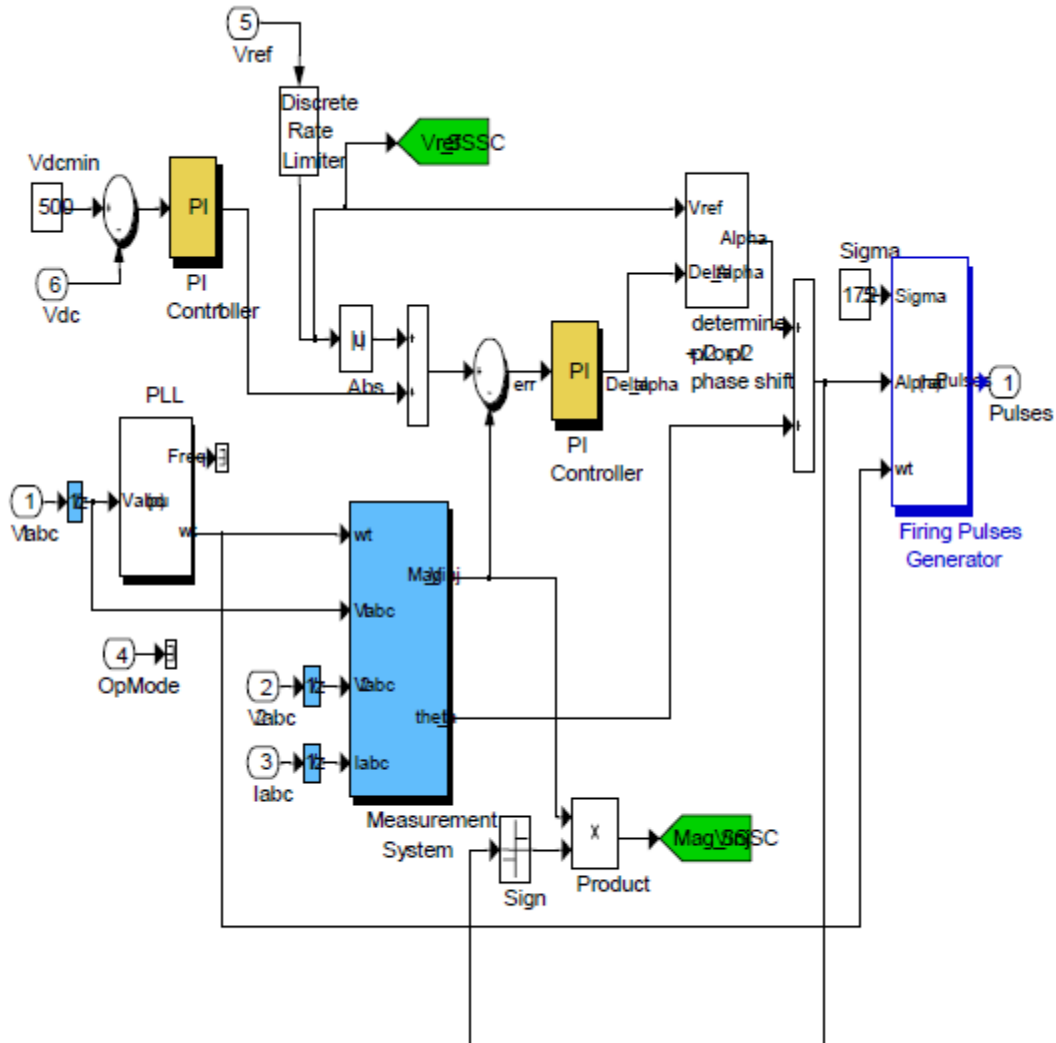


Figure 5: Simulink Sub System Block Model Of The UPFC Controller Model Showing The Phase Locked Loop & Pi Controller For Generating The Pulse Sequence For The Switching Logic for Controlling Voltage Injection Into The 330kv System During Short Circuit Situation

Both the shunt and series converters (VSC1 and VSC2) have PI (proportional integral) type of controllers that are the reference parameter values with those existing previously in the system. This shows the inputs for the PI controller's proportional gain ( $K_p$ ) and the Integral gain ( $K_i$ ). As indicated, the PI parameters ( $k_p$  and  $k_i$ ) are the input form of the MATLAB work space during the simulation as indicated by the matrix blocks ( $k_p$ ) and ( $k_i$ ). These values are the input from the work space representing PI control parameters ( $k_p$ ) ( $K_i$ ) that have been optimized by the genetic algorithm

running within the MATLAB process workspace. This enables the PI controller to send optimal control values to optimize the voltage injection by the UPFC during network disturbances.

## VII. Evaluation of System Steady State Operation with the UPFC

Figure 6 gives the steady state current profile at bus 24 near the Benue generator bus without the presence of the FACTS device in the power system and it gives the steady state signal at the same bus with the FACTS device which has proportional integral (PI) installed. As can be observed, except for the slight spike between  $t=0$  and  $t < 0.2$  seconds (greater in the case with the UPFC), there are no substantial

variations in the steady state signal structure with the FACTS device installed within the power system and with the FACTS device not installed within the system. This means that the steady state operation of the power system with the UPFC operation showed satisfactory results.

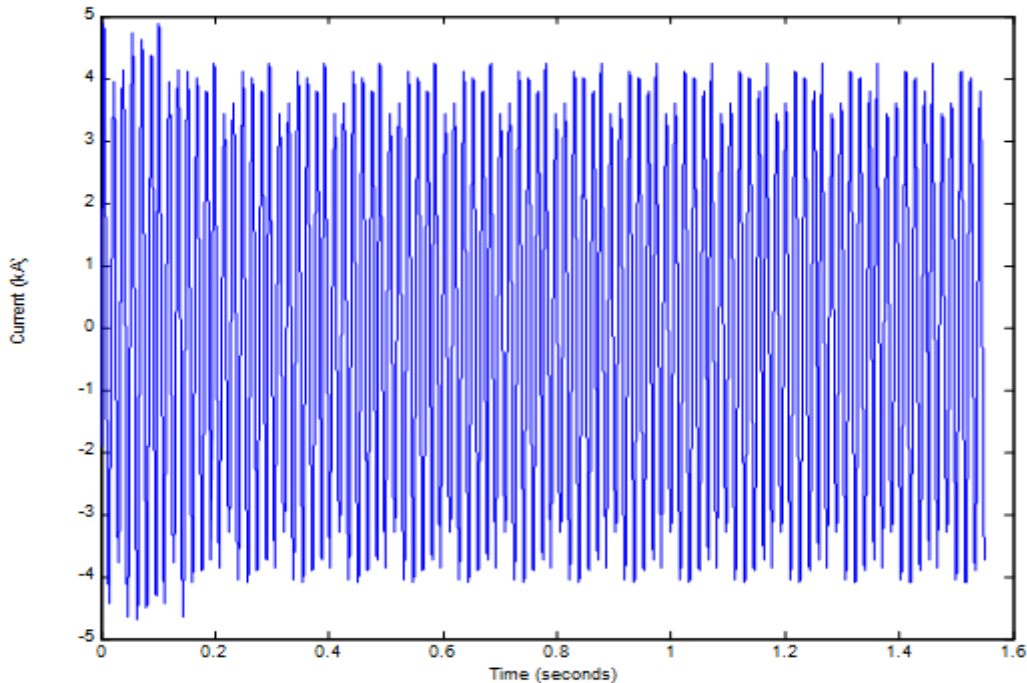


Figure 6: Power system steady state signal profile without UPFC installed

## VIII. Evaluation of System Fault State Operation with the UPFC

System response to 3 phase fault is evaluated. 3-phase fault is induced in the power system. To simulate this in SIMULINK, three-phase fault block is connected at bus 25 (i.e at Kogi) as shown in Figure 4. The SIMULINK three-phase fault block is configurable. The fault level of this block can be programmed by adjusting the fault impedance (fault resistance). This is done using the properties page of the three-phase block. To simulate different levels of faults, the fault impedance is set to  $1\Omega$ ,  $0.1\Omega$ ,  $0.01\Omega$ ,  $0.001\Omega$  and  $0.0001\Omega$ . It is important to note that the lower the fault resistance, the higher the fault MVA.

This means higher maximum short-circuit current. Fault level is proportional to the reciprocal of the fault impedance. Table 2 shows genetic algorithm parameters of a population sample, then the increase in fault current levels and the fault current limitation action by the UPFC for the different fault impedances are tabulated in Table 3.

**Table 2:** GA Parameters

Parameter	Value
Population size	30
Maximum no of generation	50
Mutation probability (PML)	0.1
Crossover Probability (PCL)	0.66
Number of bit per variable	5
Upper limit of gain	25
Lower limits	25

**Table 3:** UPFC Fault Current Limitation action for different Fault Impedances

Fault Impedance $\Omega$	power System Fault-Current rose to (KA):	UPFC reduced fault current to (KA):	percentage Fault current reduction %
1	16.5357	8.25	66.2856
0.1	28.2321	13.4464	61.1070
0.01	39.4732	18.2589	59.8640
0.001	50.8929	24.9643	55.3354
0.0001	68.4286	33.8571	53.68837
			Average reduction = 59.23%

The fault transition time of the SIMULINK three-phase fault block is set for 0.4 sec. The signal profile of the system response towards the 3-phase short-circuit current with the UPFC installed is shown in Figures 7 for fault impedance of 1  $\Omega$ .

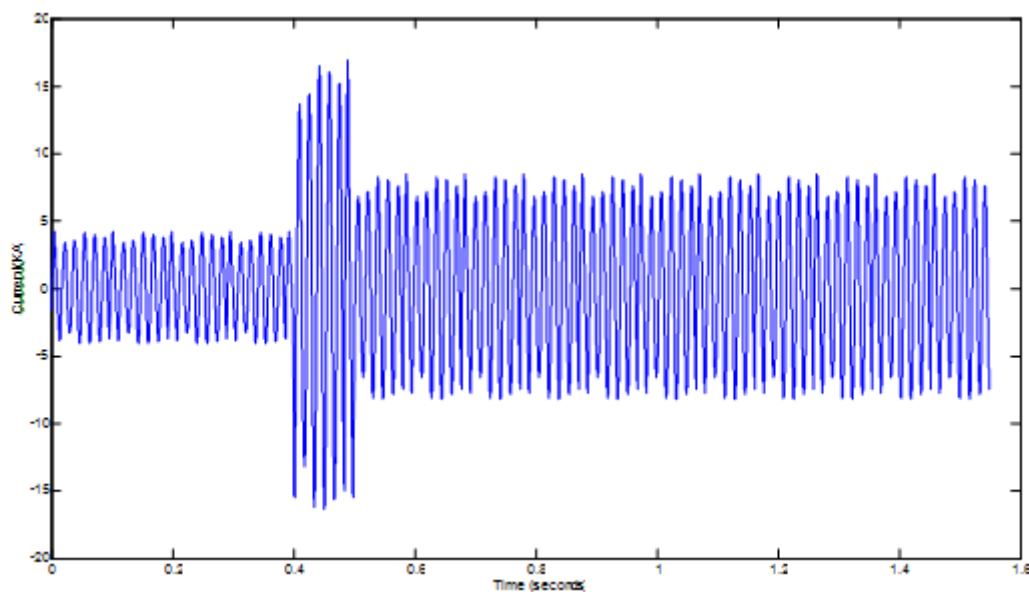


Figure: 7: Signal profile of system with UPFC installed for fault impedance of 1 ohm

In Figure 7, the fault was induced at  $t=0.4$  sec the UPFC's protective response time was activated at  $t = 0.4988$  sec.

Referring to Figure 6 the steady state current level (peak-to-peak) is around 4.0357kA from Figure 7, at fault state (fault transition system current rose to 16.5357kA. At  $t = 0.4988$  sec the high current was reduced to 8.25kA as a result of the controlled voltage injection by the UPFC.

**Before UPFC response:**

Fault current above steady state current =  $16.5357 - 4.0357 = 12.5\text{kA}$

**After UPFC response** (i.e at  $t = 0.4988$  sec):

Fault current above steady state =  $8.25 - 4.0357 = 4.2143$  kA.

This means that the UPFC reduced the short circuit current from 12.5kA to 4.2143kA. This represents a reduction of about 66.29% in relation to the peak-to-peak current value existing during the no fault condition.

The average limitation of the fault current is estimated to be 59.23%. This shows a significant reduction of the excessive fault current. This significant reduction in the short-circuit current would be very important in the protection of existing transmission assets on the power system, especially circuit breakers.

## IX. Comparison of the response time of the UPFC and the Circuit Breaker

Comparison is here made between the protection intervention response speed of the UPFC with the PI parameter optimized using genetic algorithm and that of the relay/circuit breaker pair.

Fault transition times of  $t = 0.4$  sec,  $0.5$  sec,  $0.6$  sec,  $0.7$  sec and  $0.8$  sec with fault impedance of  $1 \Omega$  is used. These five fault scenarios are simulated with the UPFC installed and with the UPFC not installed but replaced with relay/circuit breaker protection system.

The trip responses of the relay/circuit breaker protection system for the 3-phase fault transition times of  $t = 0.4, 0.5, 0.6, 0.7$  and  $0.8$  and for the same fault transition time when UPFC is installed in the network are shown in Table 4.

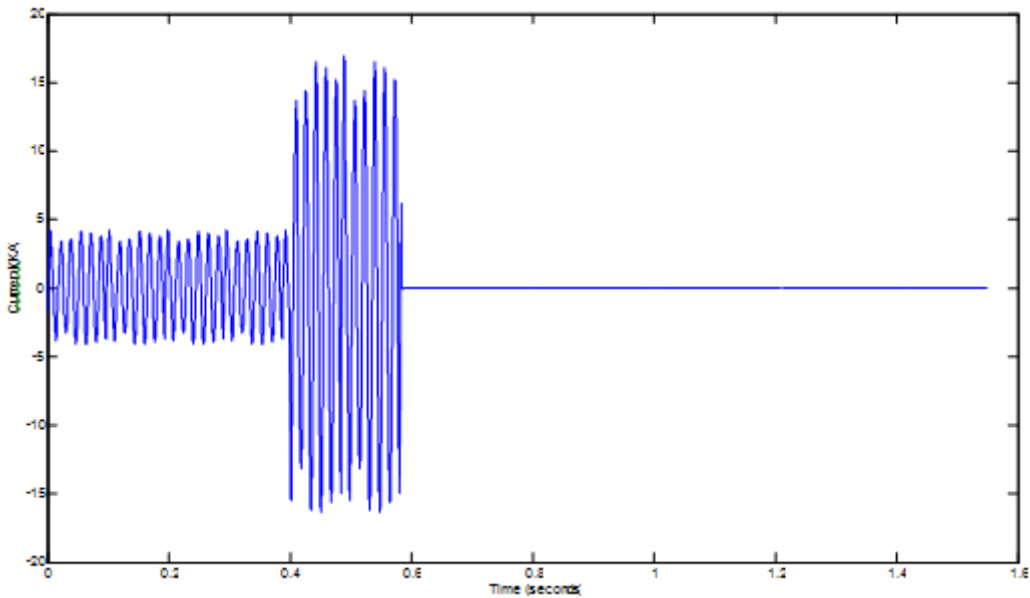


Figure 8: Signal profile of system with UPFC replaced with relay/circuit breaker protection for fault Transition time of 0.4seconds

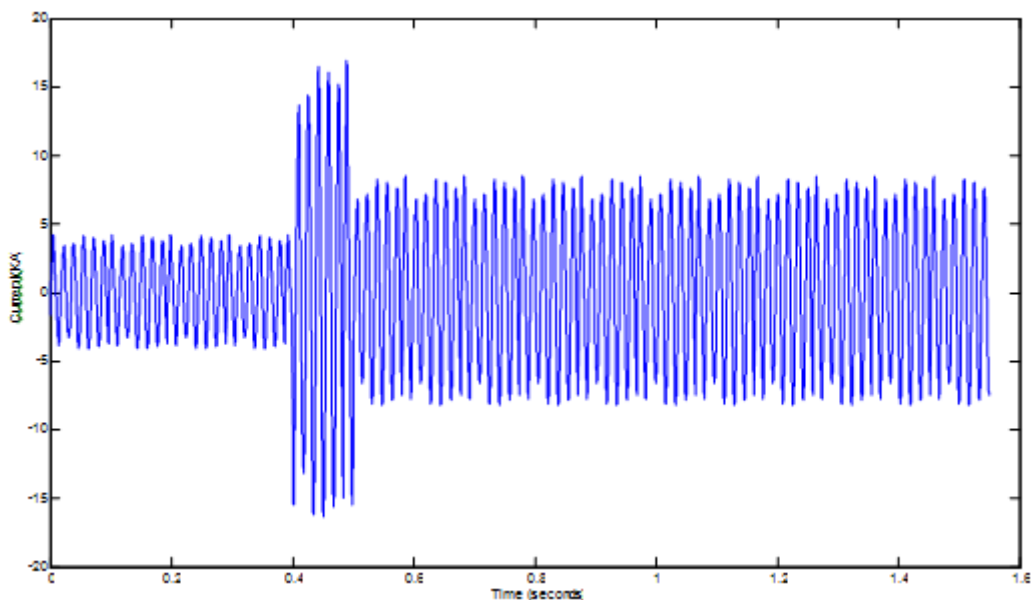


Figure 9 Signal profile of system with UPFC installed for fault transition time of 0.4 seconds

The variations of the response of the circuit breaker and the UPFC are summarized in Table 4. The estimated average response time of the circuit breaker is 0.2143 sec, while that of the UPFC is 0.01922 sec. The difference in time response is 0.19503 sec. this represents a 91% difference. This means the protective response of the facts device is faster than that of the relay/circuit breaker system by an average margin of 91%.

This wide disparity in the response of these systems can be explained from the design, support systems, configuration (level of integration with the power system) and the materials used in the manufacture of these devices. The operation time of the current transformer (CT) associated with the operation of the relay/circuit breaker introduces unavoidable delay to the operation of this conventional protection system. This is coupled with the delay with the relay (especially for non-solid state relays) plus the delay in the mechanical sub-assemblies that operate the breaker contacts. These are coupled together to introduce substantial delay compared to the fully solid state FACTS device.

The FACTS device response is almost instantaneous (with very negligible latency), since the FACTS device is fully solid state. Furthermore, the FACTS device is fully coupled with the dynamics of the power system as electronic control system. The operation of the FACTS device does not depend on any mechanical action throughout its reaction sequence.

However, this evaluation does not suggest replacing the relay/circuit breaker with FACTS devices. What is meant to show is that, in the combination of FACTS and the conventional protection system (relay/circuit breaker), the FACTS device swings faster into action than the relay/circuit breaker. This helps to quickly limit the dangerous fault current to a level that reduces excessive stress on the circuit breaker. For this improved protection combination to be effective and still maintain the quality of the power supply (without service interruption) the speed of the FACTS device should be electronic. Furthermore, the reduction of the fault current by the UPFC might be to such a level that would not require the circuit breaker to react. **Table 4:** Comparison of the fault clearing response time of the UPFC and the circuit breaker.

Fault transition time sec	UPFC	Relay/breaker trip time after fault occur (sec)	UPFC disposed time before response (sec)	Elapsed time before response (sec)
0.4	0.4988	0.5838	0.0988	0.1838
0.5	0.5960	0.723	0.096	0.223
0.6	0.6899	0.8279	0.0899	0.2279
0.7	0.7983	0.9503	0.0983	0.2503
0.8	0.8975	0.9865	0.0975	0.1865

## X. Conclusion

For the optimal control of the switching logic sequence to enable the UPFC optimize its response during fault situations, the parameters of its PI controllers have to be optimally tuned. In other words, the performance of the UPFC in reacting to short-circuit events depends on the controller parameters which are obtained by its proper tuning. Due to the shortcomings of conventional techniques used for the adjustment of the PI controller parameters, this work utilized genetic algorithm for the optimization of the PI controller parameters. Genetic algorithm is a powerful searching algorithm that mimics natural behavior based on natural genetic and natural selection. This paper developed the digital model of the Nigerian 330kV transmission system, employing UPFC as protection device. This is done to illustrate the protective fault current limitation capacity of the UPFC on high voltage systems.

The results of the simulations carried out show the effectiveness of the UPFC in reducing the level of fault currents. The current profile of the power system was observed when it was operated with UPFC and without UPFC under different short-circuit scenarios. The estimated 59.23% reduction of the level of fault current by the UPFC represents a very significant reduction of excessive current signal. Importantly, the impact of the high current reduction capability of the UPFC has significant implications for the protection of assets on the power system especially circuit breakers. It was shown that UPFC reduced the high short-circuit current from a value above the interruption capacity of circuit breakers installed in the system to a value very much below the short circuit

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interruption capacity of the circuit breakers by an appreciable margin. This would not only protect the circuit breakers from explosion, but would also help to increase the life expectancy of circuit breaker contacts between overhaul. This means reduction on maintenance runs of circuit breakers, busbars, arresters etc. It means more money being saved and higher returns on investments on transmission assets on the 330kV system.

## XI. Recommendations

It is recommended here that a pilot installation and test needs to be conducted for actual deployment of the UPFC on the Nigerian 330kV system. This would enable the distortive impact of the FACTS controller on the effective operations of the existing relays on the 330kV grid to be properly evaluated. Doing this would enable the proper distortion compensation technique to be properly worked out and validated. Furthermore, the actual deployment should consider the interpretation of the controller to Supervising Control and Data Acquisition (SCADA) system. This would both provide the platform for the intervention of power engineers and help gather operational data for optimal tuning of the PI controllers.

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