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# Design and implementation of high speed 8 bit Vedic multiplier on FPGA

[1] ANNAM ARAVIND KUMAR, [2] SK. MASTAN BASHA

[1](M.Tech) VLSI, Dept. of ECE

[2]Assistant Professor, Dept. of ECE

Priyadarshini Institute of Technology & Management

**Abstract:-** In high speed digital signal processing units arithmetic logic units, multiplier and accumulate units, the multipliers are use as the key block. A systems performance is generally determined by the speed of the multiplier since multiplier is one of the key hardware component in high performance systems such as FIR filters, digital signal processors and microprocessors etc. Vedic Mathematics is the ancient system of mathematics which has a unique technique of calculations based on 16 Sutras. With the increasing constraints on delay, more and more emphasis is being laid on design of faster multiplications. The Array multiplier, Vedic 4*4 multiplier and 8*8 multiplier are designed, then 16*16 multiplier. These adders are called compressors. Amongst these Vedic multipliers based on Vedic mathematics are presently under focus due to these being one of the fastest and low power multiplier. In this paper a 4 X 4 Vedic multiplier is designed using reversible logic gates which is efficient in terms of constant inputs, garbage outputs, quantum cost, area, speed and power. The design is simulated using Verilog. Compressor based Vedic Multipliers show considerable improvements in speed and area efficiency over the conventional ones.

**Keywords** – Multiplier, Vedic multiplier, Reversible logic, garbage output, quantum cost.

## 1. INTRODUCTION

Vedic multipliers are based on Vedic Sutras. In Sanskrit word 'Veda' stands for 'knowledge'. The Vedic mathematics has been divided into sixteen different Sutras which can be applied to any branch of mathematics like algebra, trigonometry, geometry etc. Vedic mathematics is an ancient Indian mathematical technique based on 16 sutras. The sutras of Vedic Mathematics are the software for the cosmic computer that runs this universe. Vedic Mathematics introduces the wonderful applications to Arithmetical computations, theory of numbers, compound multiplications, algebraic operations, factorizations, simple quadratic and higher order equations, simultaneous quadratic Equations, partial fractions, calculus, squaring, cubing, square root, cube root, coordinate geometry and wonderful Vedic Numerical code [1].The demand for high speed processing has been increasing as a result of expanding computer and signal processing applications. Higher throughput arithmetic operations are important to achieve the desired performance in many real-time signal and image processing applications [4]. One of the key arithmetic operations in such applications is multiplication and the development of fast multiplier circuit has been a subject of interest over decades. Reducing the time delay and power consumption are very essential requirements for many applications [2, 3]. Multiplier based on Vedic Mathematics is one of the fast and low power multiplier. Minimizing power consumption for digital systems involves optimization at all levels of the design. This optimization includes the technology used to implement the digital circuits, the circuit style and topology, the architecture for implementing the circuits and at the highest level the algorithms that are being implemented. Digital multipliers are the most commonly used components in any digital circuit design. They are fast, reliable and efficient components that are utilized to implement any operation. Depending upon the arrangement of the components, there are different types of

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multipliers available. Particular multiplier architecture is chosen based on the application.

The multipliers are the most important part of all digital signal processors; they are very important in realizing many important functions such as fast Fourier transforms and convolutions. Since a processor spends considerable amount of time in performing multiplication, an improvement in multiplication speed can greatly improve system performance. Multiplication can be implemented using many algorithms such as array, booth, carry save, and Wallace tree algorithms. Reversible logic is a promising area of study with regard to the future low power technology. It has applications in various research areas such as optical computing, low power CMOS design, DNA computing, quantum computing, thermodynamic technology, bioinformatics and nanotechnology.

### Urdhva Tiryakbhyam

In signal processing applications multiplication [5] is the most important arithmetic operation. In multiplication all the signal and data processing operations involve. In the multiplication operation as speed is always a constraint, increase in speed can be achieved by reducing the number of steps in the computation process. The speed of multiplier determines the efficiency of such a system. In any system design, the main three constraints which determine the performance of the system are speed, area and power requirement. Vedic mathematics [6] was reconstructed by Swami Bharati Krishna Tirthaji Maharaja after his eight years of research on Vedas. Vedic mathematics is mainly based on sixteen principles or word-formulae which are termed as sutras. This is a very interesting field and presents some effective algorithms which can be applied to various branches of engineering such as computing and digital signal processing. Integrating multiplication with Vedic Mathematics techniques would result in the saving of computational time. Thus, integrating Vedic mathematics for the multiplier design will enhance the speed of multiplication operation. The multiplier architecture is based on Urdhva Tiryagbhyam [7] (vertical and cross-wise algorithm) sutra. An illustration of Urdhva Tiryagbhyam sutra is shown in Figure1.

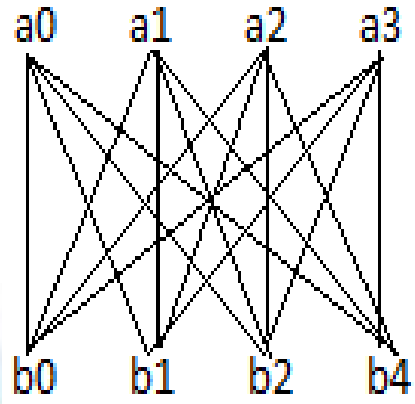


Fig 1: Illustration of Urdhva Tiryagbhyam sutra.

## 2. LITERATURE REVIEW

Energy dissipates whenever switching activity occurs in the CMOS circuits..Landauer's Principle [8] states that logical computations that are not reversible necessarily generate k*T*ln(2) joules of heat energy, where k is the Boltzmann's Constant k=1.38xl0-23 J/K, T is the absolute temperature at which the computation is performed. Although this amount of heat appears to be small, Moore's Law predicts exponential growth of heat generated due to information lost, which will be a noticeable amount of heat loss in next decade. Bennett showed that zero energy dissipation would be possible only if the network consists of reversible logic gates, Thus reversibility will become an essential property in future circuit design technologies. Reversible circuits are those circuits that do not loose information. Reversible computation in a system can be performed only when the system comprises of reversible gates.

In paper [9] H. Thapliyal and M.B. Srinivas designed the multiplier using two units; one is the partial product generation unit constructed using Fredkin gates and other the summing unit constructed using 4x4 TSG gates. [7] has proposed a design of reversible multiplier which makes use of Peres gate for generation of partial products as compared to [10], which uses Fredkin gates. For the construction of adders the HNG gate was devised. [10] Proposes low quantum cost realization of reversible multipliers which mainly uses Peres full adder gate (PFAG) for its design. It also uses Peres gates for the generation of partial products.

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## 3. VEDIC MATHEMATICS

Vedic mathematics is part of four Vedas (books of wisdom). It is part of Sthapatya- Veda (book on civil engineering and architecture), which is an upa-veda (supplement) of Atharva Veda. It gives explanation of several mathematical terms including arithmetic, geometry (plane, co-ordinate), trigonometry, quadratic equations, factorization and even calculus. Swamiji constructed 16 sutras (formulae) and 16 Upa sutras (sub formulae) after extensive research in Atharva Veda. Obviously these formulae are not to be found in present text of Atharva Veda because these formulae were constructed by Swamiji himself. Vedic mathematics is not only a mathematical wonder but also it is logical. That's why it has such a degree of eminence which cannot be disapproved. Due these phenomenal characteristics, Vedic maths has already crossed the boundaries of India and has become an interesting topic of research abroad. Vedic maths deals with several basic as well as complex mathematical operations. Especially, methods of basic arithmetic are extremely simple and powerful [2, 3]. The word "Vedic" is derived from the word "Veda" which means the store-house of all knowledge. Vedic mathematics is mainly based on 16 Sutras (or aphorisms) dealing with various branches of mathematics like arithmetic, algebra, geometry etc[11]. These Sutras along with their brief meanings are enlisted below alphabetically.

1. (Anurupye) Shunyamany at – If one is in ratio, the other is zero.
2. Chalana-Kalanabyham – Differences and Similarities.
3. Ekadhikina Purvena – By one more than the previous One.
4. Ekanyunena Purvena – By one less than the previous one.
5. Gunakasamuchyah – The factors of the sum is equal to the sum of the factors.
6. Gunitasamuchyah – The product of the sum is equal to the sum of the product.
7. Nikhilam Navatashcaramam Dashatah – All from 9 and last from 10.
8. Paraavartya Yojayet – Transpose and adjust.
9. Puranapuranabyham – By the completion or noncompletion.
10. Sankalana- vyavakalanabhyam – By addition and by subtraction
11. Shesanyankena Charamena – The remainders by the last digit.
12. Shunyam Saamyasamuccaye – When the sum is the same that sum is zero.
13. Sopaantyadvayamantyam – The ultimate and twice the penultimate.
14. Urdhva-tiryagbhyam – Vertically and crosswise.
15. Vyashtisamanstih – Part and Whole.
16. Yaavadunam – Whatever the extent of its deficiency.

## 4.DESIGN OF VEDIC MULTIPLIER

### 4.1. Urdhva –Triyagbhyam(Vertically and Crosswise)

Urdhva tiryakbhyam Sutra is a general multiplication formula applicable to all cases of multiplication. It literally means "Vertically and Crosswise". To illustrate this multiplication scheme, let us consider the multiplication of two decimal numbers (5498 × 2314). The conventional methods already know to us will require 16 multiplications and 15 additions.

The numbers to be multiplied are written on two consecutive sides of the square as shown in the figure. The square is divided into rows and columns where each row/column corresponds to one of the digit of either a multiplier or a multiplicand. Thus, each digit of the multiplier has a small box common to a digit of the multiplicand. These small boxes are partitioned into two halves by the crosswise lines. Each digit of the multiplier is then independently multiplied with every digit of the multiplicand and the two-digit product is written in the common box. All the digits lying on a crosswise dotted line are added to the previous carry. The least significant digit of the obtained number acts as the result digit and the rest as the carry for the next step.

Here, "Urdhva Tiryakbhyam Sutra" or "Vertically and Crosswise Algorithm"[12] for multiplication has been effectively used to develop digital multiplier architecture. This algorithm is quite different from the traditional method of multiplication, which is to add and shift the partial products.

## 5. VEDIC MULTIPLIER

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The "Urdhva Tiryagbhyam" Sutra is a general multiplication formula applicable to all cases of multiplication such as binary, hex, decimal and octal. The Sanskrit word "Urdhva" means "Vertically" and "Tiryagbhyam" means "crosswise". Fig 4 shows an example of Urdhva Tiryagbhyam.

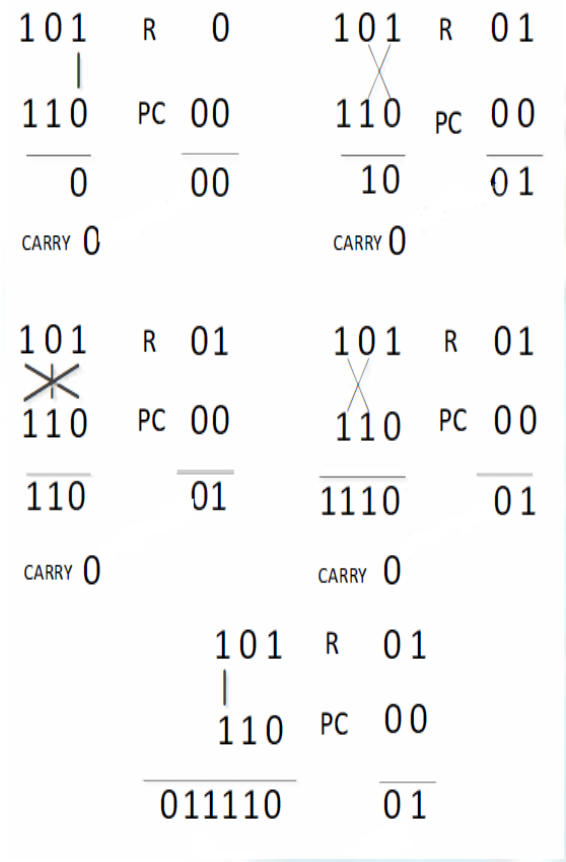


Fig 2: Example of Urdhva Tiryagbhyam algorithm

The partial products are generated parallel and concurrent additions of the partial products are done using this algorithm. Because of this the speed of the multiplier is increased considerably when compared to other techniques.

### Low Power and High Speed Vedic Multiplier

The adder architecture consisted of two parts- Carry generator and Carry propagator[15]. These parts generates the N+1th carry bit with the help of the initial carry and thus this does not need to wait for Nth carry to propagate. Since the carry is generated in advance in this adder, it decreases the carry propagation time and thus this architecture improves the operational speed. A comparison of propagation delay, power dissipation and the number of transistors, made between this architecture, Array multiplier[13] and the Booth radix 4 multiplier, shows that the Vedic multiplier with carry Look ahead adder is better than the other two in speed and power dissipation. But the number of transistors used increases in the proposed architecture.

## 6.VEDIC MULTIPLIER USING REVERSIBLE LOGIC

The 2 X 2 Urdhva Tiryagbhyam multiplier using conventional logic will have 4 outputs. The logical expressions are given below.
q0= a0.b0
ql= (a1.b0) xor (a0.bl)
q2= (a0.al.b0.bl) xor (al.bl)
q3= a0.al.b0.bl

The reversible logic implementation of the above expressions requires four peres gate and one Feynmen (CNOT) gate. The reversible logic implementation of 2 X 2 UT multiplier is shown in the Fig 3. The quantum cost of the 2X2 Urdhva Tiryakbhayam Multiplier[14] is found to be 21. The number of garbage outputs is 9 and number of constant inputs is 4.
The partial products generated using the 2 X 2 UT multiplier are need to be added using the four bit adder.. The four bit ripple carry adder unit using HNG gate is shown in the Fig 4.

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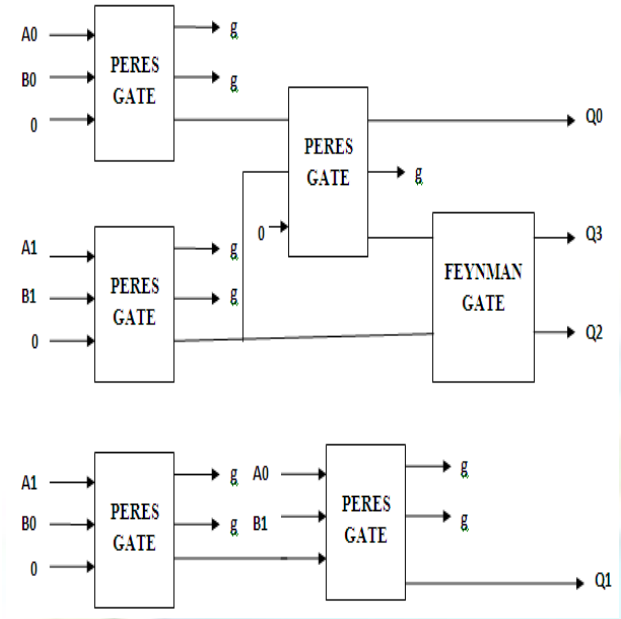



Fig 3. A 2 X 2 Urdhva Tiryagbhyam multiplier Unit

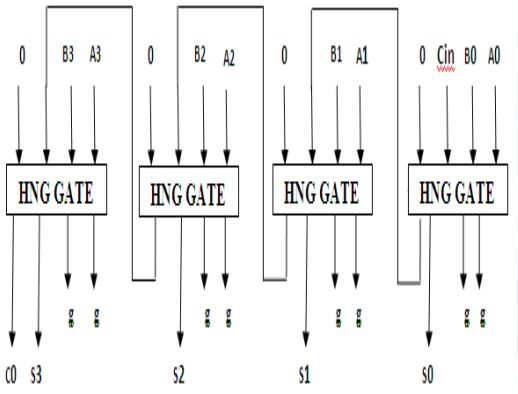


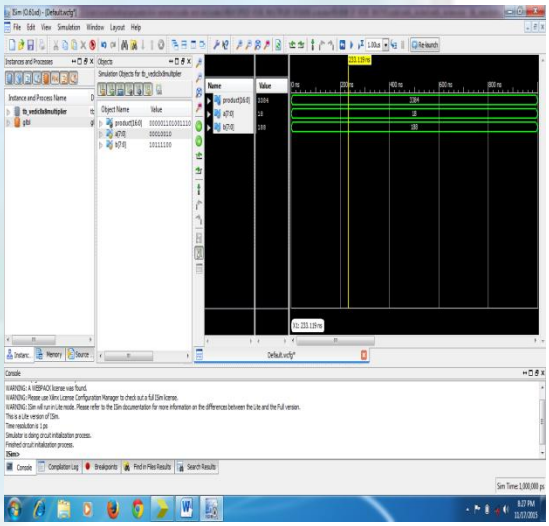

Fig . 4 Four bit ripple carry adder using HNG gate

## 7. RESULTS

VEDIC MULTIPLIER 8BIT

RTL SCHEMATIC


OUTPUT



VEDIC MULTIPLIER_CLLA 8BIT

RTL SCHEMATIC

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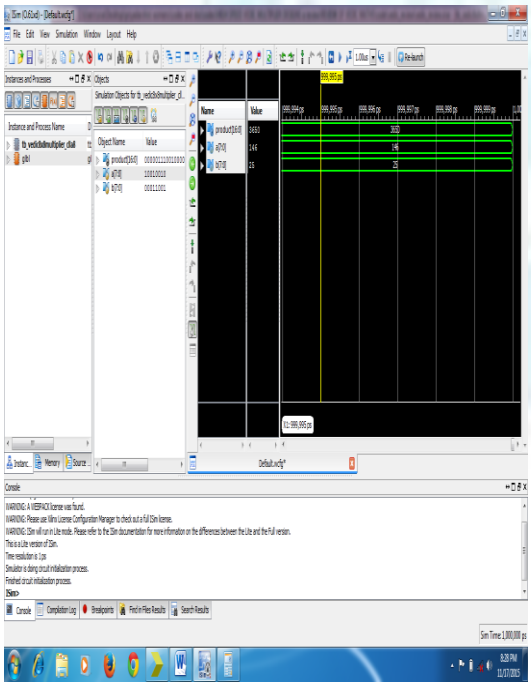
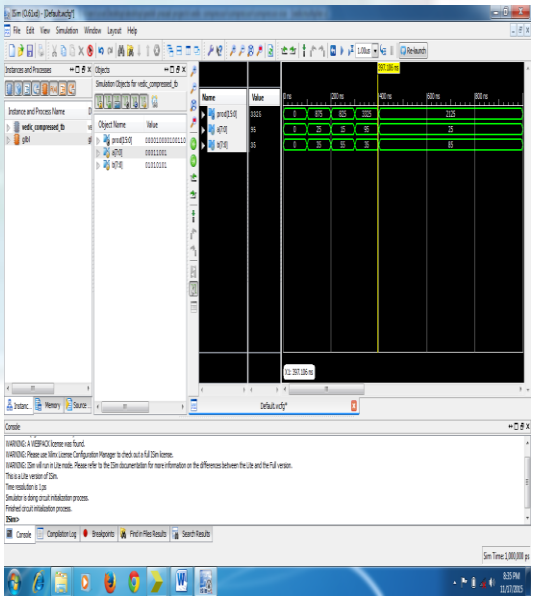
OUTPUT



VEDIC MULTIPLIER COMPRESSOR 8BIT

RTL SCHEMATIC


OUTPUT



VEDIC MULTIPLIER CSA 8BIT

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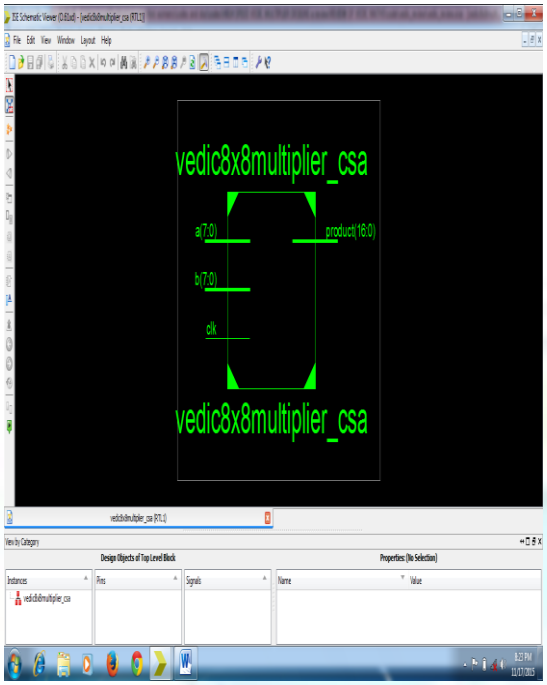
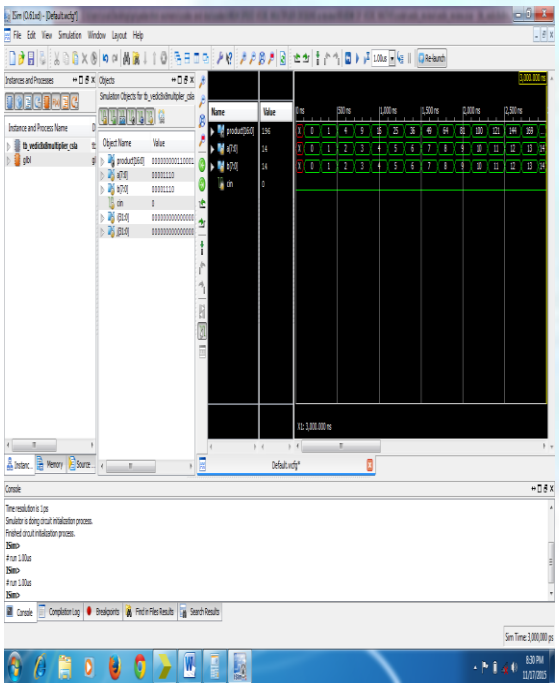
RTL SCHEMATIC




OUTPUT



## 8. CONCLUSION

Vedic Multiplier is seen to be efficient in speed, power and area in digital designs with respect to other multipliers. Considering all the designs of it discussed above, we can conclude that the Compressor based Vedic multiplier with Urdhva Tiryakbhyam sutra is seen as a promising technique in terms of speed and area. First 2X2 UT multiplier is designed using Peres gate and Feynmen gate. The ripple carry adders which were required for adding the partial products were constructed using HNG gates. This design has high speed, smaller area and less power consumption when compared with other reversible logic multipliers.

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