Circuit for Revisable Quantum Multiplier Implementation of Adders with Reversible Logic

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Abstract: Programmable reversible logic is gain wide consideration as a logic design style for modern nanotechnology and quantum computing with minimal impact on circuit heat generation in improved computer architecture and arithmetic logic unit designs. In this paper, a 2*2 Swap gate which is a reduced implementation in terms of quantum cost and delay to the previous Swap gate is presented. Then, a novel 3*3 programmable UPG gate capable of calculating the universal logic calculations is presented and verified, and its advantages over the Toffoli and Peres gates are discussed. The UPG is then implemented in a reduced design for calculating n-bit AND, n-bit OR and n-bit ZERO calculations. Then, two 3*3 RMUX gates capable of multiplexing two input values with reduced quantum cost and delay compared to the previously existing Fredkin gate is presented and verified. Next, a novel 4*4 reversible programmable RC gate capable of nine unique logical calculations at low cost and delay is presented and verified. The UPG and RC are implemented in the design of novel sequential and tree-based comparators. These designs are compared to previously existing designs, and their advantages in terms of cost and delay are analyzed.Then, the RMUX is used to improve a reversible SRAM cell we previously presented. The memory cell and comparator are implemented in the design of a Min/Max Comparator device.

Keywords: Reversible Logic, Quantum cost, Garbage output, Xilinx ISE 14.7

1. INTRODUCTION

Normal Combinational Logic Circuits dissipate heat for every bit of information lost during their operation. Due to this, the recovery of a piece of information once lost is completely impossible. However, if the same circuit is constructed using the Reversible Logic Gates, not only is the recovery possible but also the dissipation of heat reduced. [1]In the 1960s, R. Landauer demonstrated that even with high technology systems when designed using Irreversible hardware result in high energy dissipation and efficiency loss. He showed that the loss per bit of information exchange dissipates KT.ln2 Joules of energy where K is Boltzmann Constant and T the Absolute Temperature at which the operation is performed. [2]Later in 1973, Bennett showed that this amount of energy loss can be overcome if the circuit is designed using the Reversible Logic technique. With the number of chip components doubling every 18

months, as per Moore's Law, the Irreversible Technologies would dissipate a lot of heat and reduce circuit life. It is here the Reversible Logic comes into action in not only recovering the lost information but also dissipating less heat. A Reversible Logic Gate is an n-input, n-output device with n-to-n Mapping, which helps determining the outputs from the inputs and vice versa. Wherever necessary, extra outputs can be added to make the output count equal to that of the input. The main challenges are diminishing Number of Gates, Memory Usage, Delay and Quantum Cost.

2. LITERATURE SURVEY:

In this section, detailed literature review is done that aims to review the critical points of current works. Here the information collected about researches and innovations carried out on the related technologies has

been done. This section will highlight the recent trends and innovations in the concerned technology.

Landauer [1] determined that, the amount of energy dissipated for the loss of each bit of information is at least kTln2 (where k is the Boltzmann constant i.e. 3 *10^12 joule at room temperature). During any computation the intermediate bits used to compute the final result are lost, this loss of bits is one of the main reason for the power dissipation.

C. H. Bennett [2] in 1973 discovered that the power dissipation in any device can be made zero or negligible if the computation is done using reversible model. The theory is proved with turing machine which is a symbolic model for computation developed by Turing. Bennett also showed that the computations that are performed on irreversible or classical machine can be performed with same efficiency on the reversible machine. Based on the above concept the research on the reversibility was started in 1980's.

Soolmaz Abbasalizadeh[4] has designed 4-Bit Comparator Based on Reversible Logic Gates. Here he explained that reversible logic has been considered as one of the promising practical strategies for power-efficient computing. In fact, when the inputs can't be recovered from circuit's outputs, information loss appears. Reversible logic circuits can handle this issue. In this logic, one to one mapping exists between the inputs and outputs. The number of inputs and outputs are equal, and inputs can be recovered from outputs

3. REVERSIBLE LOGIC

Reversible logic is a successful computing design pattern which presents a method to construct a computer with no heat generation. Reversible Logic Gate is an n-input, n-output device that provides n-to-n Mapping between input and output, which helps determining the outputs from the inputs and vice versa. The input that is added to an NXN function to make it reversible is called constant input (CI)[3]. Garbage outputs (GO) are the outputs of the reversible circuit that do not contribute to reversible logic realization. Any output that will not take part in the realization of circuit in which the gate used will be considered as garbage outputs. Quantum cost (QC) refers to the cost of the circuit in terms of the cost of a primitive gate. This can be computed knowing the number of primitive reversible logic gates (1*1 or 2*2) required to realize the circuit. These parameters have to

be reduced while designing a reversible circuit. Some of the major constraint of the reversible logic synthesis are that do not allow fan-out's, and also feedback from gate outputs to inputs is not allowed. A reversible circuit should have minimum number of reversible logic gates. Wherever required, extra outputs can be added to make the output count equal to input. The main challenges are reduction in Number of Gates, Memory Usage, Delay and Quantum Cost.

3.1 HNG Gate
It is a 4x4 gate and its logic circuit is as shown in the figure1. It has quantum cost six. It is used for designing adders like ripple carry adder. It reduces the garbage and gate counts by producing the sum and carry in the same gate.

3.2 Toffoli Gate
It is a 3x3 gate and its logic circuit is as shown in the figure1. It has quantum cost two. It is used to realize various Boolean functions such as XOR, AND.

3.3 Peres Gate
It is a 3x3 gate and its logic circuit is as shown in the figure1. It has quantum cost four. It is used to realize various Boolean functions such as XOR, AND.

3.4 Fredkin Gate
It is a 3x3 gate and its logic circuit is as shown in the figure1. It has quantum cost five. It can be used to implement a Multiplexer.

3.5 TSG Gate

It is a 4x4 gate and its logic circuit is shown in figure1. It can be used to implement adders like carry skip adder and carry bypass adder. Quantum cost is not specified by the author so it is unknown.

The important design constraints of the reversible logic circuits are
1. Reversible logic circuit should have minimum quantum cost.
2. The design can be optimized so as to produce minimum number of garbage outputs.
3. The reversible logic circuits must use minimum number of constant inputs.
4. The reversible logic circuits must use minimum number of reversible gates

4. ADDER TOPOLOGIES

This section presents the design of adder topology. In this work the following adder structures are used: Ripple Carry Adder Carry Save Add Carry Skip Adder Carry Bypass Adder

4.1 Ripple Carry Adder

The ripple carry adder is constructed by cascading full adders (FA) blocks[4] in series. Single full adder is responsible for the addition of two binary digits at any stage of the ripple carry adder. The carryout of one stage is fed directly to the carry-in of the proceeding stage. Even though this is a simple adder and can be used to add unrestricted bit length numbers, it is however not very efficient when large bit numbers are used. One of the most severe drawbacks of this adder is that the delay increases linearly with the bit length.
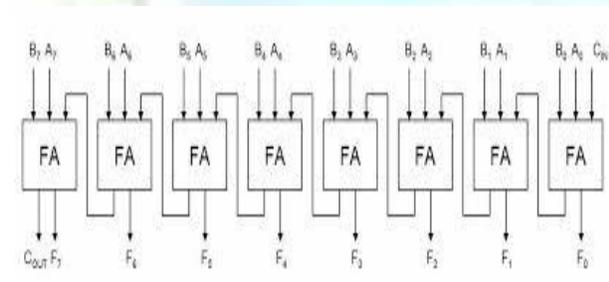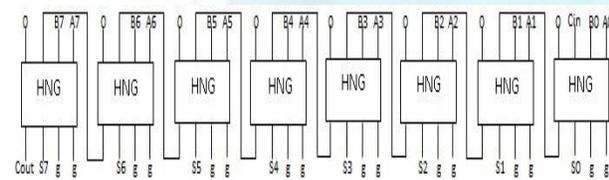

Fig.1. Conventional 8-Bit Ripple Carry Adder

Fig.2 Bit Ripple Carry Adder Using Reversible Logic

4.2 Carry Skip Adder

A carry-skip adder consists of a simple ripple carry-adder with a special speed up carry chain called a skip chain. Carry skip adder[6] is better in speed compared to ripple carry adder when addition of large number of bits take place. Carry skip adder has provides a good compromise in delay, along with a simple and regular layout. This chain defines the distribution of ripple carry[15] blocks, which forms the skip adder. A carry-skip adder is designed to speed up a wide adder by aiding the propagation of a carry bit around a portion of the entire adder. The conventional 8 bit carry skip adder is shown in the figure 3 in reversible carry skip adder all the full adders are replaced by TSG[5] gate, AND gates are replaced with Peres Gates and OR gates are replaced with FRG gates .
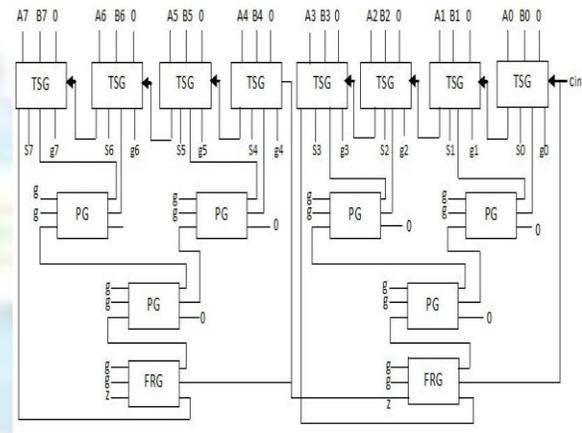

Fig.3-Bit Reversible Carry Skip Adder

4.3 Carry save Adder

The carry-save adder reduces the addition of 3 numbers to the addition of 2 numbers. The propagation delay is 3 gates regardless of the number of bits. The carry-save[14] unit comprises of n full adders, each of which computes a single sum and carries bit based solely on the corresponding bits of the three input numbers. The entire sum can then be computed by shifting the carry sequence left by one place and appending a 0 to the front (most significant bit) of the partial sum sequence and adding this sequence with RCA[7] produces the resulting n + 1-bit value. This procedure can be continued indefinitely, adding an input for each level of full adders, without any intermediate carry propagation. These stages can be arranged in a binary tree structure, with cumulative delay logarithmic in the number of inputs to be added, and invariant of the number of bits per input. The conventional 8 bit carry save adder is shown in the figure6. in reversible carry save adder all the full adders are replaced by HNG gate and all the half adders are replaced with the . Reversible 8 bit carry save adder is shown in figure 4. The quantum cost is

78, constant input(CI) s 16,garbage output(GO)is 23 and number of gates(NG) is 16.
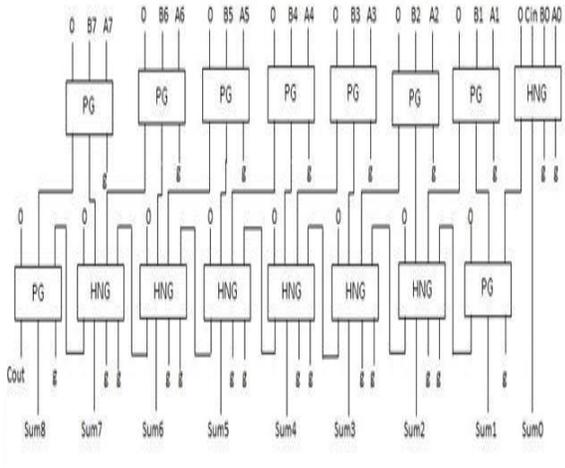

Fig.4-Bit Reversible Carry save Adder

4.4 Carry Bypass Adder

As in a ripple-carry adder, every full adder cell has to wait for the incoming carry before an outgoing carry can be generated. This dependency can be eliminated by introducing an additional bypass (skip) to speed up the operation of the adder. An incoming carry $C_{i,0}=1$ propagates through complete adder chain and causes an outgoing carry $C_{0,7}=1$ under the conditions that all propagation signals are 1. LFSR systems are typically designed either using field programmable gate arrays (FPGAs)[8][9] or digital signal processors (DSPs).

While this leads to a working system which are flexible in nature, then the system speed is limited by the fact that FPGAs and DSPs are all general-purpose systems. By using VLSI techniques in order to come out with the design of a LFSR, the throughput can be increased and the LFSR is easily integrated into a system design since the area needed is minimal. This research presents three different automated techniques for implementing LFSR as well as D flip flop so that the layout area will be minimized as well as the power consumption will be lower. Nisha Haridas and M Nirmala Devi[8]. explained that pattern generation is the most important module in a BIST. Out of many test pattern generators (TPG) explored for the BIST, linear feedback shift register (LFSR) are widely used due to their ability to produce highly random patterns. Various

improvements over the basic forms of the LFSR are available. In the current study, in the selection of the appropriate LFSR[10] for a given benchmark circuit is analyzed.
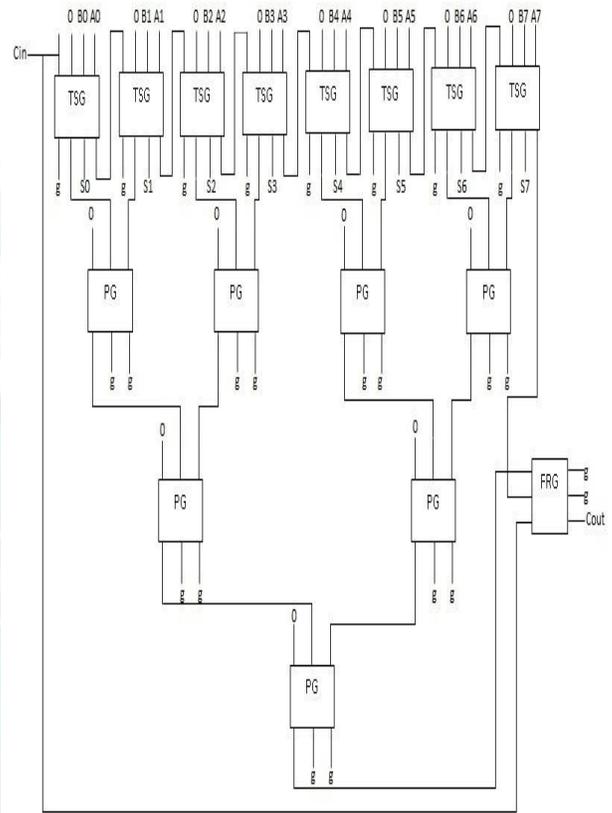

Fig.5-Bit Reversible Carry Bypass Adder

5. SYSTEM DESIGN:

Classical Computing Machines using irreversible logic gates unavoidably generates heat. This is due to the fact that each loss of one bit of information is accompanied by an increase of the environment's entropy by an amount K ln2, where k is Boltzmann's constant. In turn this means that an amount of thermal energy equal to KT ln2 is transferred to the environment[13], having a temperature T. According to Landauer's principle it is possible to construct a computer that dissipates an arbitrarily small amount of heat.

A necessary condition is that no information is thrown away. Therefore, logical reversibility is a necessary condition. Here the LFSR using the reversible rates will be designed in order to reduce the power dissipation.

LFSR is a shift register that, when clocked, advances the signal through the register from one bit to the next most-significant bit. Some of the outputs are combined in exclusive-OR[12] configuration to form a feedback mechanism.

Linear feedback shift registers are extremely good pseudorandom pattern generators. When the outputs of the flip-flops are loaded with a seed value (anything except all 0s, which would cause the LFSR[11] to produce all 0 patterns) and when the LFSR is clocked, it will generate a pseudorandom pattern of 1s and 0s. Note that, the only signal necessary to generate the test patterns is the clock.. It is done by considering the various factors such as selection of characteristic polynomial and seed to obtain high fault coverage, minimize invalid patterns, area overhead and time taken to generate the patterns.

The leakage current flowing through a stack of series connected transistors reduces when more than one transistor of the stack is turned OFF. The effect is called as "Stacking Effect". When two or more transistors that are switched low or OFF, and are grouped that are put one on top of each other then they dissipate less leakage power than a single transistor that is turned OFF which reduces the leakage current. Reverse body biasing (RBB) can be used to dynamically raise the threshold voltage during standby mode, thereby reducing the leakage power. Reverse bias is applied to the body of the devices and threshold voltages can be changed which is due to the body effect. For example, biasing an NMOS device body with a voltage lower than Ground, or biasing a PMOS device body with the voltage higher than Vcc will increase the threshold voltage which results in reduction in leakage current.

6. CONCLUSION:

The main aim is to design and implement the reversible logic based LFSR. As a prior work, literature survey has been done. It is observed that, there are many innovative ideas and solutions are put forth for the power optimization by many researchers such as reverse body bias, transistor stacking, LFSR design with parallel architecture, pipelining and retiming algorithms and reversible logic. So observing all these white papers, one can ensure that reversible logic would be one of the better solutions for the designing of LFSR in order to generate the pseudo random signals, with the better optimization of the power.

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