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Square and Cube Architecture using Less Complex and Low Power Architectures

[1]BELLAM SREEKANYA,[2]K.RAKESH

[1](M.Tech) VLSI, Dept. of ECE

[2]Assistant Professor, Dept. of ECE

Priyadarshini Institute of Technology & Science for Women

Abstract: In this paper we are going to explore the importance of the design of a Low power and less area square and cube architectures using Vedic sutra , the optimized multiplier are having regular, less complex and parallel structure in design thus this kind of algorithm and its designs used to design square and cube circuit using Vedic sutras over and over again times square and cube are the most sustained on operations in several digital signal processing applications and computation can be condensed using Radix8 and the overall processor performance can be improved for numerous applications.

Keywords- DWT, Radix8, Parallel Structure, VEDIC, Urdhva Tiryagbhyam, Anurupyena Sutra, Modified Booth,

I. INTRODUCTION

Square and cube are frequently performed functions in most of the DSP systems. Square and cube are special cases of multiplication. Square and cube architectures forms the heart of the different DSP operations like Image Compression, Decoding, Demodulation, Adaptive Filtering, Least Mean Squaring etc., and also have numerous applications as mentioned in [1] such as cryptography, computation of Euclidean distance among pixels for a graphics processor or in rectangular to polar conversions in several signal processing circuits where full precision results are not required. Traditionally, square and cube were performed using multiplier itself. As the applications evolved demand for the high speed processing increased, special attention was given for square and cube function [9-11]. Most important feature of the Vedic mathematics [2] is its coherence, entire system is wisely interrelated and unified. Simple Squaring Scheme can easily be reversed to produce one-line Square Roots. These methods are very easy to understand. In this paper algorithms and architectures used to design square and cube of a binary number is explored and to create a circuit using the Vedic Sutras. Often Times Square and cube are the most time-consuming operations in many of digital signal processing applications and computation can be reduced using the Vedic sutras and the overall processor performance can be improved for many applications [8]. Therefore, the goal is to create a square and cube architectures that is comparable in speed, power and area than a design using an standard multiplier. The motivation behind this work is to explore the design and implementation of Square and Cube architectures for low power.

II. RELATED WORKS

A high speed multiplier design (ASIC) using Vedic mathematics was presented in [1]. The idea for designing the multiplier and adder unit was adopted from ancient Indian mathematics "Vedas". Based on those formulae, the partial products and sums are generated in single step which reduces carry propagation from LSB to MSB. The implementation of the Vedic mathematics and their application to the complex multiplier ensured substantial reduction of propagation delay in comparison with Distributed Array (DA) based architecture and parallel adder based implementation which are most commonly used architectures. The implementation of the Vedic algorithms in DSP is highlighted in [2]. In this, multiplication process based on Vedic mathematics and its implementation on 8085 and 8086 microprocessors were shown. A study of processing time conventional multipliers for 8085 and 8086 was done. It was shown that there is an appreciable saving in the proc essing time of the Vedic multiplier as when compared to that of a conventional multiplier. A time, area, power efficient multiplier architecture using

Vedic mathematics was shown in [3]. In this a comparative study of the array multiplier, Carry save multiplier, Wallace tree multiplier, Booth multiplier and Vedic multiplier was done in detail.

III. VEDIC MATHEMATICS

A. Square Architecture Dwandwa Yoga

The Dwandwa Yoga or 'duplex combination' can be used for general purpose squaring. The square of a number can be calculated by using the duplex,, D property of dwandwa yoga. According to duplex property, for an even number of elements the result is taken as twice the product of the outermost pair and then twice the product of the next outermost pair and so on till no pairs are left. For an odd number of elements, there is one bit left itself in the middle and this enters as its square along with the product elements.

A. Vedic Mathematics Sutras

This list of sutra is taken from the book Vedic Mathematics [2], which includes a full list of the 16 main sutras. The following are the 16 main sutras or formulae of Vedic math and their meaning in English. Ekadhikena Purvena: One more than the previous Nikhilam Navatascharamam Dastah: All from nine and last from ten Urdhwa-tiryagbhyam: Criss-cross Paravartya Yojayet: Transpose and adjust Sunyam Samyasamuchchaye: When the samuchchaya is the same, the samuchchaya is zero, and i.e. it should be equated to zero. (Anurupye) Sunyamanyat: If one is in ratio, the other one is zero. Sankalana-vyavkalanabhyam: By addition and by subtraction Puranpuranabhyam: By completion or non-completion Chalana-Kalanabhyam: Differential Yavdunam: Double Vyastisamastih: Use the average Sesanyankena Charmena: The remainders by the last digit Sopantyadyaymantyam: The ultimate & twice the penultimate Ekanyunena Purven: One less than the previous Gunitasamuchachayah: The product of the sum of coefficients in the factors Gunaksamuchchayah: When a quadratic expression is product of the binomials then its first differential is sum of the two factors

B. Vedic Mathematics Sub-Sutras Anurupyena:

Proportionately Sisyate Sesasamjnah: Remainder remains constant Adyamadyenantyamantyena: First by first and last by last Kevalaih Saptakam Gunyat: In case of seven our multiplicand should be 143 Vestanam: Osculation Yavdunam Tavdunam: Whatever the extent of its deficiency, lessen it still further to that very extent Yavdunam Tavdunam Varganchya Yojayet: Whatever the extents of its deficiency lessen it still further to that very extent; and also set up the square of that deficiency. Antyayordasakepi: Whose last digits together total 10 and whose previous part is exactly the same Antyayoreva: Only the last terms Samuchchyagunitah: The sum of the coefficients in the product Lopanasthapanabhyam: By alternate elimination and retention Vilokanam: By observation Gunitsamuchchayah Samuchchayagunitah: The product of sum of the coefficients in the factors is equal to the sum of the coefficients in the product.

B. Proposed Squaring Algorithm

In the proposed algorithm the square of a binary number can be calculated based on the duplex property of dwandwa yoga logic. This squaring algorithm has all the advantages as it is quite smaller than the array, booth and vedic multiplier. This multiplication algorithm is also advantageous over urdhava tiryakbhyam multiplication algorithm as it requires less number of computations over urdhava tiryakbhyam for the same number of bits. Square Architecture using dwandwa yoga property of urdhvatiryagbhyam sutra. Yavadunam Sutra is used for Squaring , is limited to the number which are near the base 10,100 etc., The "Ekadhikena Purvena Sutra" is used for Squaring, is limited to number which ends with digit 5 only. The other method "Dwandwa Yoga" or Duplex is used in two different senses. The first one is by squaring and the second one is by cross multiplication. It is used in both the senses (a 2, b 2 and 2ab) In order to calculate the square of a number "Duplex" D property of Urdhva Tiryagbhyam is used. In the Duplex, take twice the product of the outermost pair, and then add twice the product of the next outermost pair, and so on till no pairs are left. When there are odd number of bits in the original sequence there is one bit left by itself in the middle, and this enters as its square. Thus for
987654321, D= 2 * (9 * 1)+2 * (8 * 2)+2 * (7 * 3)+ 2 * (6 * 4)+ 5 * 5=165.
Further, the Duplex can be explained as follows
For a 1 bit number D is its square.
For a 2 bit number D is twice their product
For a 3 bit number D is twice the product of the outer pair +the square of the middle bit.
For a 4 bit number D is twice the product of the outer pair +twice the product of the inner pair.
Thus D (1) = 1 * 1;
D (11) =2 * 1 * 1;
D (101) =2 * 1 * 1+0 * 0;
D (1011) =2 * 1 * 1+2 * 1 * 0;

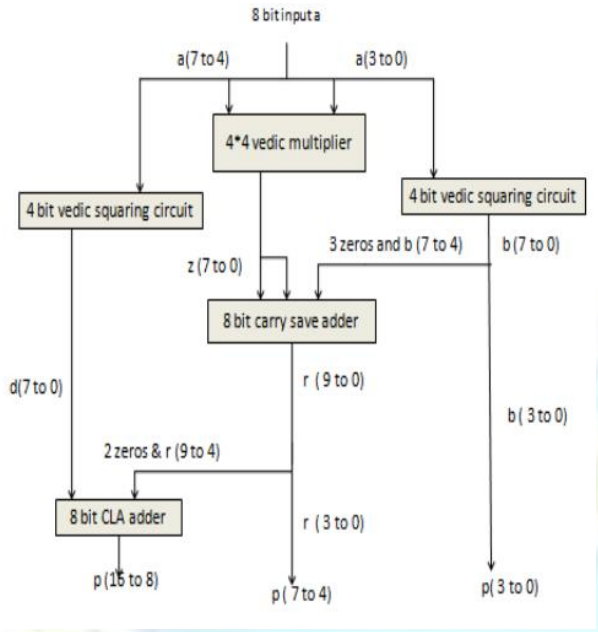

Fig.1. Block diagram 8 bit squaring circuit

The Vedic square has all the advantages of the Vedic multiplier. Further, it is quite faster and smaller than the array, Booth and proposed Vedic multiplier.

IV. CUBE ARCHITECTURE

Cube of two digit decimal number can be calculated by using Anurupyena sutra of Vedic mathematics. Example:

$24^3 =$	2^3	$2^2 * 4$	$4^2 * 2$	4^3
	8	16	32	64
	8	16 * 3	32*3	64
	8	48	96	64

Now add them up with carry over excess digits from right to left. 8+5=13 | 48+ 10= 58=8 |96+6=102=2 | 4 243 = 13824

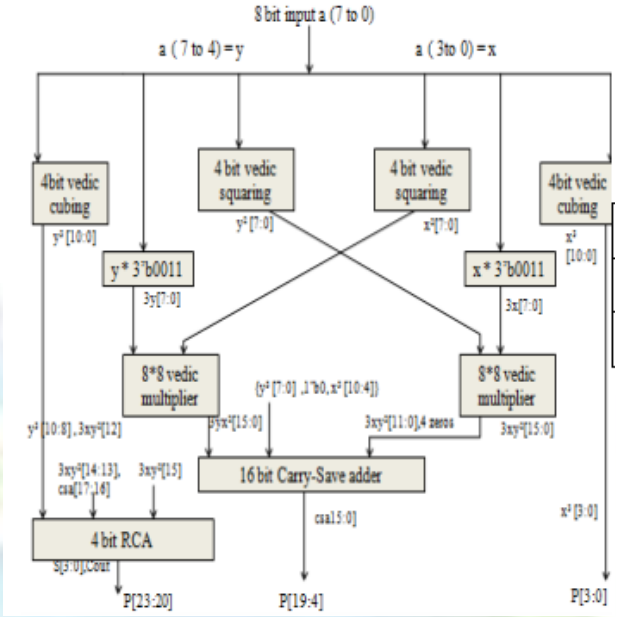

Fig 2: 8-bit Vedic cubing architecture

A. Anurupyena Sutra Meaning Various Forms (Proportion/Ratio), Eg: 2 can be written as 2 OR 4/2 OR 16/8 OR 1*2 OR 0.5*4, etc. Note that the first row can also be expressed as writing the numbers from the cube of the first digit to the cube of the second digit such that the numbers in between form the same ratio with respect to each other. In other words, the numbers in the first row are in geometric progression from the cube of the first digit to the cube of the second digit. In fact the constant ratio of the geometric progression is the same as the ratio between the first and second digits of the number to be cubed. Also note that the procedure above is a direct result of the algebraic identity that (a + b) 3 = a 3 + 3a 2 b + 3ab 2 + b 3. The first line contains the terms a 3, a 2 b, ab 2 and b 3 . The second row contains the remaining 2a 2 b and 2ab 2 (double of the middle two terms of the first row).

B. Booth Encoding Algorithm

Booth's multiplication algorithm is a multiplication algorithm that multiplies two signed binary numbers in two's complement notation. The algorithm was invented by Andrew Donald Booth in 1950 while doing research on crystallography at Birkbeck College in Bloomsbury, London. Booth used desk calculators that were faster at shifting than adding and created the algorithm to increase their speed. Booth's algorithm is of interest in the study of computer

C. Radix-8 Modified Booth

Modified Booth multiplier consists of Modified Booth Recorder (MBR). MBR have two parts, i.e., Booth Encoder (BE) and Booth Selector (BS). The basic operation of BE is to decode the multiplier signal and output will be used by BS to generate the partial product. The partial products are then, added with the Wallace tree adders, similar to the carry save adder approach. The last row of carry and sum output is added together by carry look- a head adder with the carry skewed to the left b y position. Radix-8 Booth recoding applies the same algorithm as that of Radix-4, but now we take quartets of bits instead of triplets. Each quartet is codified as a signed digit using below Table, Radix-8 algorithm reduces the number of partial products to n/3, where n is the number of multiplier bits. Thus it allows a time gain in the partial products summation.

V.CONCLUSION

In this paper a new binary number squaring and cubing algorithm have been proposed. The duplex property is used to perform the squaring; cubing calculations are more deeply studied and designed using vedic sutras. With the help of this algorithm large computations can be handled significantly with less delay. It is therefore seen that the Vedic multipliers are much faster than the conventional multipliers. The algorithms of Vedic mathematics are much more efficient than that of conventional mathematics.

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