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SYSTEM EVALUATION OF 32 BIT UNNSIGNED MULTIPLER USING CLAA AND CSLA.

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Abstract:- In this paper deals with the comparison of the VLSI design of the carry look-ahead adder (CLAA) based 32-bit signed and unsigned integer multiplier. Multiplication is a fundamental operation in most signal processing algorithms. Multipliers have large area, long latency and consume considerable power. Therefore low-power multiplier design has been an important part in low- power VLSI system design. In computational circuits the adders plays a key role in arithmetic operations. Adders like Ripple carry adder, Carry look ahead adder, Carry select adder, Carry skip adder and carry save adder etc. In this paper, a high performance and low power 32bit unsigned multiplier is proposed using adders. The CLAA based multiplier and CSLA based multiplier uses the same delay for multiplication operation.

Keywords – CLAA,CSLA,Delay,Area, Array Multiplier

1. INTRODUCTION

The design of low power, low area and high performance logic systems are most essential in VLSI system design. The digital systems such as embedded systems, Digital signal processing (DSP), Data process unit and Communication network the arithmetic operations like addition, subtraction; multiplication and division are mostly used and plays a key role in various applications. In electronics, the adder is a digital circuit. The adder can be used to perform the addition of binary numbers. In many computers and different type of processors and controllers, adders are not only used in the arithmetic logic unit and not only perform the addition operation. They are used to calculate addresses, registers and different type of operations. Multiplication is one of the basic arithmetic operations. Multiplication operation is also called as a adding and shifting method. Multiplication operation involves two methods one is Generation of partial products and another one is summation. The speed of multiplication is mainly depends on the Partial product generation and/or summation. The multiplication speed will be high when the generation of partial products is less. In this, we are going to implement the Two 32-bit unsigned multipliers using adders. . In many processors Carry select adder is used to perform the fast arithmetic operations. The carry propagation delay time is very high in Ripple carry adder. To overcome this problem Carry look ahead adder is proposed. This type of adder does not require the carry propagation step by step. The CLAA and CSLA adders have the similarity properties. For the multiplication process the both adders (CLAA & CSLA) will have the nearly same delay speed. Here The Two 32-bit unsigned multipliers multiplies (N*N) and gives the 64 bit (2N) output.

Considered while designing multipliers. Due to device portability miniaturization of device should be high and power consumption should be low. High-speed data path logic systems are one of the most substantial areas of research in VLSI system design. In digital adders, the speed of addition is limited by the time required to propagate a carry through the adder. The sum for each bit position in an elementary adder is

generated sequentially only after the previous bit position has been summed and a carry propagated into the next position. Ripple carry adders exhibits the most compact design but the slowest in speed. Whereas carry look ahead is the fastest one but consumes more area. Carry select adders act as a compromise between the two adders. A new concept of hybrid adders is presented to speed up addition process. The CSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input Cin = 0and Cin = 0, then the final sum and carry are selected by the multiplexers (mux).In this project we are going to compare the performance of different adders implemented to the multipliers based on area and time needed for calculation. On comparison with the carry look-ahead adder (CLAA) based multiplier the area of calculation of the carry select adder (CSLA) based multiplier is smaller and better with nearly same delay time. Here we are dealing with the comparison in the bit range of n*n (32*32) as input and 2n(64) bit output. Multiplication is a mathematical operation that at its simplest is an abbreviated process of adding an integer a specified number of times. Multiplication is the fundamental arithmetic operation important in several processors and digital signal processing systems. Multiplication of two k bit number needed multi operand addition process that can be realized in k cycles of shifting and addition with hardware, firmware or software. Multiplication based operations such as multiply and accumulate (MAC) and inner product are among some of the frequently used intensive arithmetic functions currently implemented in many digital signal processing (DSP) applications such as convolution, fast Fourier transform(FFT),filtering and in microprocessors in its arithmetic and logic unit. Portable multimedia and digital signal processing (DSP) systems, which typically require low power consumption, short design cycle, and flexible processing ability, have become increasingly popular over the past few years. As many multimedia and DSP applications are highly multiplication intensive so that the performance and power consumption of these systems are

2. ADDERS

In electronics, an adder is digital circuit which is used to perform the addition of binary digits. In VLSI system design using adders we are increasing the erformance of the module. In this section we will review the different types of adders and their characteristics and performance.

2.1 Half adder

The half adder adds two binary inputs a,b and its have the two binary outputs Sum and carry. The logic diagram of half adder is shown in below figure1.

$$Sum = A \oplus B$$
$$Carry = AB$$

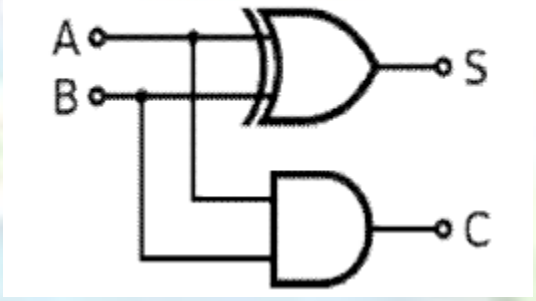

Fig 1: Half adder logic diagram

2.2 Full adder

The full adder adds three binary inputs a,b,cin and its have the two binary outputs Sum and Carry. The logic diagram of the full adder is shown in below figure2.

$$Sum = A \oplus B \oplus C$$
$$Carry = AB+BC+CA$$

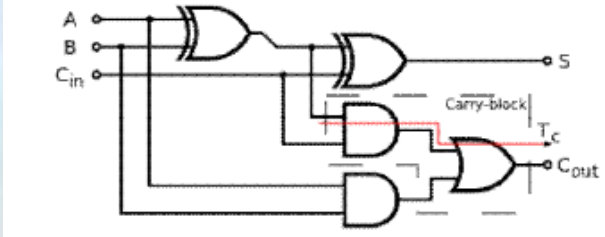

Fig2: Full adder logic design

2.3 Ripple carry adder

Ripple carry adder is a combination of multiple full adders to add N-bit numbers. Here we are dealing with the 4-Bit Ripple carry adder. This 4-Bit ripple carry adder is the combination of four full adders. Each full adder has the three binary inputs and two binary outputs Sum and Carry. Each full adder output Carry is input to the next full adder this kind of adder is called as the Ripple carry adder. The block diagram of 4-bit Ripple carry adder is shown in below figure3.

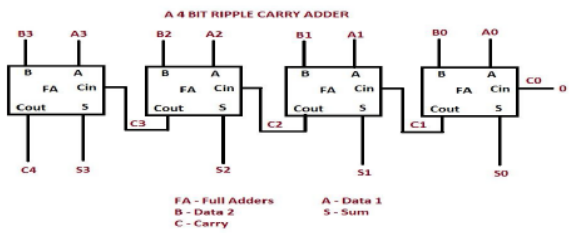

Figure 3: 4-bit Ripple carry adder

2.4 Carry look ahead adder

In the adders the performance of the adder is mainly based on the carry propagation. The ripple carry Adder calculates the carry bits along with the sum so the performance of the ripple carry adder is slow but it takes the low power. To overcome this problem we are designing the carry look ahead adder. The carry look ahead adder first calculates the all carry bits after its calculates the sum bits. The carry propagation (P) and Carry generation (G) is given as the outputs sum and carry is given as

$$S_i = P_i \oplus C_{i-1}$$
$$C_{i+1} = G_i + P_i C_i$$

The final carry output is given as

$$C_{i+1} = Gi + PiG_{i-1} + PiP_{i-1}G_{i-2} + \ldots\ldots. P_iP_{i-1}\ldots.P_2P_1G_0 + PiP_{i-1} \ldots.P_1P_0C_0.$$

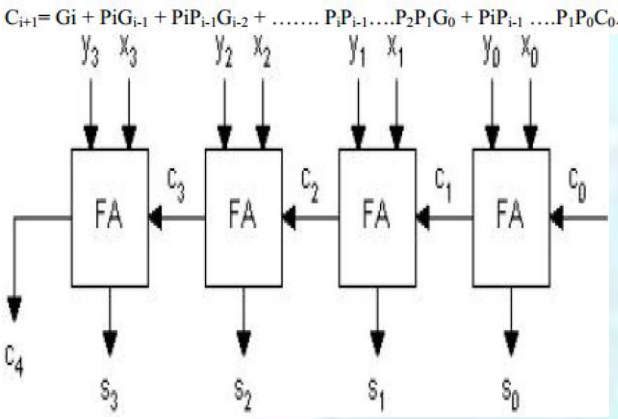

Fig 4: Carry looks ahead adder

2.5 Carry select adder

Generally the CSLA have the two ripple carry adder stages and multiplexer. Carry select adder selects the correct result using multiplexer with single stage or multiple stage. For two stages of ripple carry adders we have the two outputs (2 sums, 2 carrys). The correct result will be selected by the multiplexer and speed will be high when comparing with the different adders.

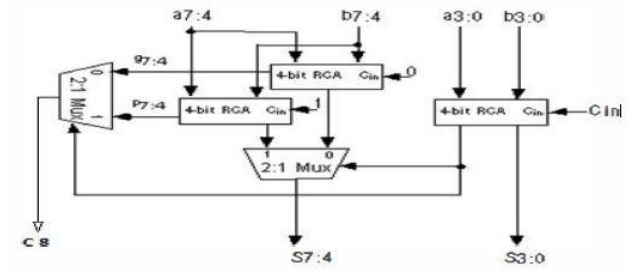

Fig 5. Carry select adder

3. UNSIGNED MULTIPLIER

The multiplier is one of the hardware key blocks in Digital signal processing techniques. The multiplier involves generation of partial products and summation. The n-bit multiplier multiplies with the n-bit multiplier and it gives the final product term is a 2n bit value. The two 32 bit unsigned multipliers multiplication output will be shown in below figure6.

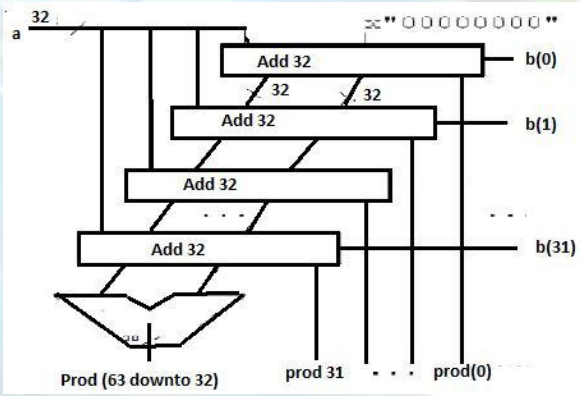

Fig 5. Unsigned Multiplier

4. SIMULATION RESULTS

This project has been developed by using Verilog language. The two unsigned 32 bit multiplier simulation results are presented in this section. In this, RTL view of top module and design summary is shown in the below figures. We have performed simulation results using the Modals 10.1b and synthesized by Xilinx 14.2.Here we are designing the two 32-bit unsigned multipliers using CLAA and CSLA. CLAA and CSLA multipliers have the 32 binary inputs and 32 binary outputs. Both multipliers binary outputs multiply and it gives as 64-bit product term according to the multiplication operation.

The HDL simulation of the two multipliers is presented in this section. In this, waveforms, timing diagrams, the design summary and the power analysis for both the CLAA and CSLA based multipliers are shown in the figures. The HDL code for both multipliers, using CLAA and CSLA, are generated. The HDL model has been developed using Modelsim6.4b.The multipliers use two 32-bit values.

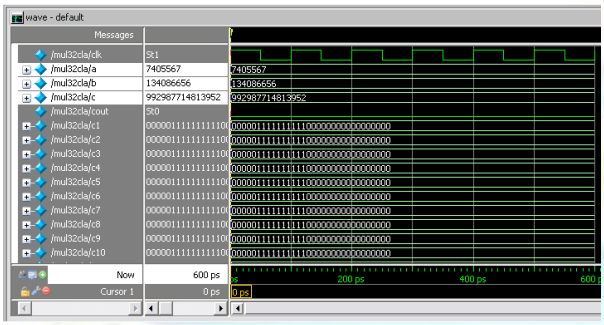

Fig 6:32 bit multiplier using cla

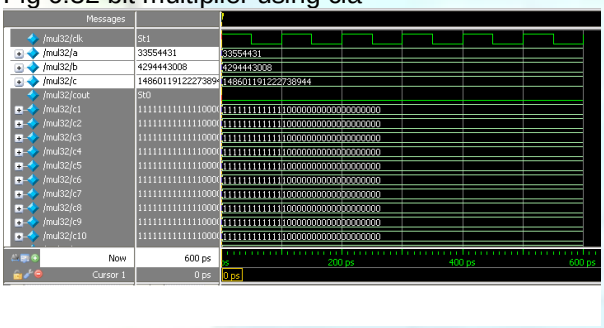

Fig 7:32bit multiplier using CSLA

Performance Analysis of Adders In this analysis table shown in figure, the delay time is nearly same, the area and the area delay product of CSLA based multiplier is reduced to 06 % when compared to CLAA based multiplier.

ADDERS	DELAY (ns)	FREQUENCY (MHz)	MEMORY (MB)
Carry Save Adder	21.666	46.155	146.896
Carry Skip Adder	19.668	50.844	151.688
Carry Select Adder	19.061	52.4631	151.156

The power performance analysis for the CLAA and CSLA based multipliers are represented in the form of the diagram shown in figure and the table above. Here the power dissipation are approximately same for both CLAA & CSLA.

	Total power	Dynamic power	Static power	Thermal power
CLAA	72.52	4.82	46.36	21.33
CSLA	72.53	4.83	46.35	21.36

5. CONCLUSION

The Design of high speed 32bit unsigned multiplier using adders is proposed. Simulation and synthesis of high speed 32bit unsigned multiplier using CLAA and CSLA has been done in Xilinx using Verilog Hardware Description Language. The CSLA increases the performance of the multiplier.

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