

# Design and Simulation of High Speed Low Power CMOS Comparator

<sup>1</sup>A.Rajeswari, <sup>2</sup>T.Venkatarao

*1(M.Tech) DECS Branch, Department of ECE*

*2 Asst.Professor, Department of ECE*

*Vignan's Nirula Institute of Technology & Science for Women  
Pedapalakaluru, Guntur, Andhra Pradesh, India*

**Abstract:**-In high-speed high-resolution analog to digital converters, comparators have a key role in quality of performance. High power consumption and delay is one of the drawbacks of these circuits which can be reduced by using suitable architectures. Many versions of comparator are proposed to achieve desirable output in sub-micron and deep sub-micron design technologies. Back to-back inverter in the latch stage is replaced with dual-input single output differential amplifier. This topology completely removes the noise that is present in the input. The structure shows lower power dissipation and higher speed than the conventional comparators. The circuit is simulated with 0.8V DC supply voltage and 250 MHz clock frequency. The proposed circuit analyses the Inverter based differential amplifier design compared to double tail comparator is a less delay and controls the power dissipation. Finally output results shown by using T-Spice tool in TSMC018

**Keywords** – CMOS comparator, low power, High Speed, Analog-to-Digital Converter and Tanner EDA tool

## 1. INTRODUCTION

The rapidly growing market of portable electronic systems such as wireless communication devices, consumer electronics or battery-powered medical devices increases the demand for developing low voltage and low-power circuit techniques and building blocks. One such application where low power, high resolution and high speed are required is analog-to-digital converters (ADCs) as a key components in mixed-signal integrated circuits. Recent ADC applications are used increasingly in digital data reading fields, such as hard disk drives, digital video discs and local area networks. High sampling speed is required in all of these applications, best solution for high speed, low latency operations is flash architecture but performance degrades as number of comparator increases. Alternative to this folding CMOS comparator which reduces number of comparators but performance degrades due to process variation. A novel circuit for low power, low cost, high speed CMOS ADC is general successive approximation ADC is presented where

comparators plays a key role. Greatly affect the overall performance of the device. One such application where low power dissipation, low noise, high speed, less hysteresis, less Offset voltage are required is Analog to Digital converters for mobile and portable devices. The performance limiting blocks in such ADCs are typically inter-stage gain amplifiers and comparators. The accuracy of such comparators, which is defined by its offset, along with power consumption, speed is of keen interest in achieving overall higher performance of ADCs. In the past, pre-amplifier based comparators have been used for ADC architectures such as flash and pipeline. The main drawback of pre-amplifier based comparators is the more offset voltage. To overcome this problem, dynamic comparators are often used that make a comparison once every clock period and require much less offset voltage. However, these dynamic comparators suffer from large power dissipation compared to pre-amplifier based comparators. The main problem with all these dynamic comparators is the output signal of the latch stage is fluctuating during clock transition. This is happening due to the presence of noise in input

terminals. In this paper we have designed all type of comparators.

## 2. OVERVIEW OF COMPARATOR

A comparator is a circuit that provides a high Boolean output if the differential input is positive and a low Boolean output if the differential input is negative. High gain amplifiers are often used as comparators since the outputs of most amplifiers naturally clip at high and low levels when overdriven. Since comparators are usually not used with feedback, there is not a need for compensation so neither the area reduction or speed reduction penalty is incurred. Since feedback is not used, higher-order amplifiers such as cascades can be used to increase the gain of a comparator to arbitrarily high levels. If over-driven amplifiers are used for comparators, the power dissipation of these types of comparators is often high.

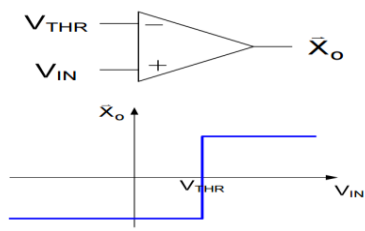


Fig.1 Comparator

Some comparators are clocked and only provide an output after the transition of the clock. The value of the input to a clocked comparator is only of concern in a short time interval around the clock transition. The speed of clocked comparators can be very high and the power dissipation of clocked comparators can be very low. Clocked comparators are often called Dynamic Comparators. Regenerative feedback is often used in dynamic comparators and occasionally in non-clocked comparators. Dynamic comparators are widely used in the design of high-speed ADCs.

### 2.1. CONVENTIONAL DYNAMIC COMPARATOR

The circuit diagram of the conventional dynamic comparator widely used in A/D converters, with high input impedance, rail-to-rail output swing, and no static power consumption is shown in Fig. 2[1]. The operation of the comparator is as follows.

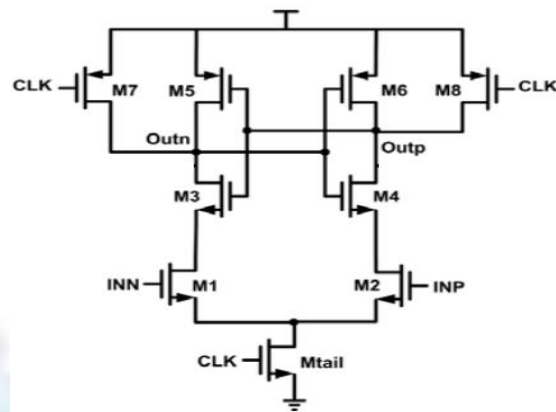


Fig.2. Circuit diagram of conventional dynamic Comparator

During the reset phase when  $CLK = 0$  and  $M_{tail}$  is off, reset transistors ( $M7-M8$ ) pull both output nodes  $Outn$  and  $Outp$  to  $VDD$  to define a start condition and to have a valid logical level during reset. In the comparison phase, when  $CLK = VDD$ , transistors  $M7$  and  $M8$  are off, and  $M_{tail}$  is on. Output voltages ( $Outp$ ,  $Outn$ ), which had been pre-charged to  $VDD$ , start to discharge with different discharging rates depending on the corresponding input voltage ( $INN/INP$ ). Assuming the case where  $V_{INP} > V_{INN}$ ,  $Outp$  discharges faster than  $Outn$ , hence when  $Outp$  (discharged by transistor  $M2$  drain current), falls down to  $VDD - |V_{thp}|$  before  $Outn$  (discharged by transistor  $M1$  drain current), the corresponding pMOS transistor ( $M5$ ) will turn on initiating the latch regeneration caused by back-to-back inverters ( $M3, M5$  and  $M4, M6$ ). Thus,  $Outn$  pulls to  $VDD$  and  $Outp$  discharges to ground. If  $V_{INP} < V_{INN}$ , the circuit works vice versa.

### 2.2. DOUBLE TAIL COMPARATOR

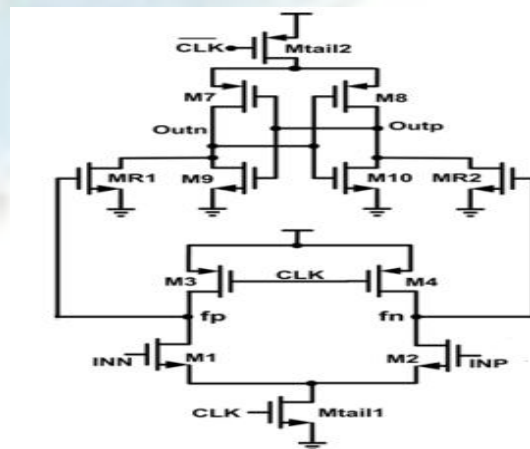


Fig.3 Circuit diagram of double tail comparator

A Circuit diagram of double tail comparator is shown in Fig3 [10]. During reset phase (CLK = 0, Mtail1, and Mtail2 are off), transistors M3-M4 pre-charge fn and fp nodes to VDD, which in turn causes transistors MR1 and MR2 to discharge the output nodes to ground. It is also called as precharge phase. During decision-making phase (CLK = VDD, Mtail1 and Mtail2 turn on), M3-M4 turn off and voltages at nodes fn and fp start to drop with the rate defined by  $i_{tail1}/C_{fn}(p)$  and on top of this, an input-dependent differential voltage  $V_{fn}(p)$  will build up. The intermediate stage formed by MR1 and MR2 passes  $V_{fn}(p)$  to the cross coupled inverters and also provides a good shielding between input and output, resulting in reduced value of power and delay.

**2.3. DOUBLE TAIL COMPARATOR WITH CONTROLLED TRANSISTORS**

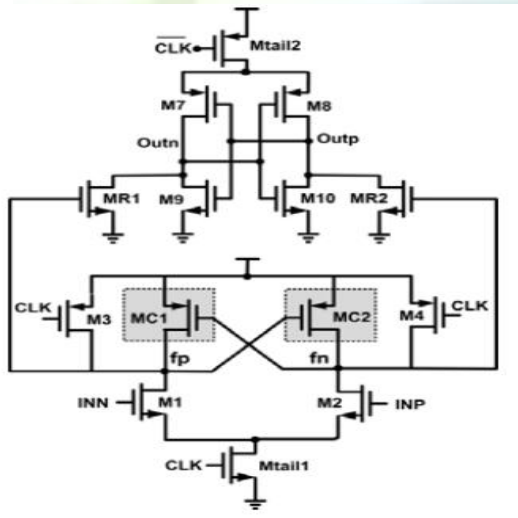


Fig.4 Circuit diagram of Comparator with controlled transistors

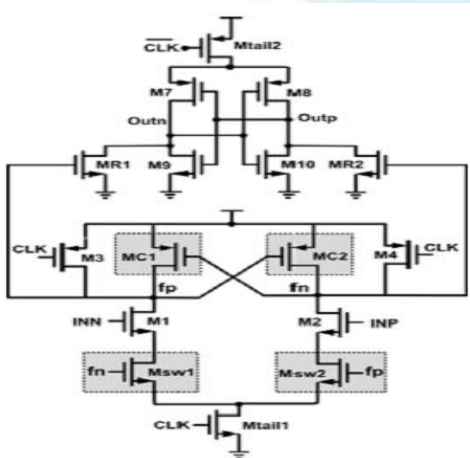


Fig.5.Circuit diagram of Comparator with Switched transistors

The operation of the comparator is as follows. During reset phase (CLK = 0, Mtail1 and Mtail2 are off, avoiding static power), M3 and M4 pulls both fn and fp nodes to VDD, hence transistor Mc1 and Mc2 are cut off. Intermediate stage transistors, MR1 and MR2, reset both latch outputs to ground. During decision-making phase (CLK = VDD, Mtail1, and Mtail2 are on), transistors M3 and M4 turn off. Furthermore, at the beginning of this phase, the control transistors are still off (since fn and fp are about VDD). Thus, fn and fp start to drop with different rates according to the input voltages. Suppose  $V_{INP} > V_{INN}$ , thus fn drops faster than fp, (since M2 provides more current than M1). As long as fn continues falling, the corresponding pMOS control transistor (Mc1 in this case) starts to turn on, pulling fp node back to the VDD; so another control transistor (Mc2) remains off, allowing fn to be discharged completely.

In other words, unlike conventional double-tail dynamic comparator, in which  $V_{fn}/fp$  is just a function of input transistor trans-conductance and input voltage difference, in the proposed structure as soon as the comparator detects that for instance node fn discharges faster, a pMOS transistor (Mc1) turns on, pulling the other node fp back to the VDD. Therefore by the time passing, the difference between fn and fp ( $V_{fn}/fp$ ) increases in an exponential manner, leading to the reduction of latch regeneration time. Despite the effectiveness of the proposed idea, one of the points which should be considered is that in this circuit, when one of the control transistors (e.g., Mc1) turns on, a current from VDD is drawn to the ground via input and tail transistor (e.g., Mc1, M1, and Mtail1), resulting in static power consumption. To overcome this issue, two NMOS switches are used below the input transistors [Msw1 and Msw2, as shown in Fig.4 and 5].

**3. PROPOSED INVERTER BASED DIFFERENTIAL AMPLIFIER**

The new approach of analog circuit techniques that is compatible with future CMOS technologies. There are several important advantages of this approach. First, the need to develop expensive CMOS technologies with lower threshold voltages is avoided. Secondly, high efficiency dc-dc converters are not required. Thirdly, circuit techniques that permit low voltage operation with large thresholds offer the potential for more fully utilizing the technology at higher voltages and at lower voltages if, in

fact, low threshold technologies do become standard technologies.

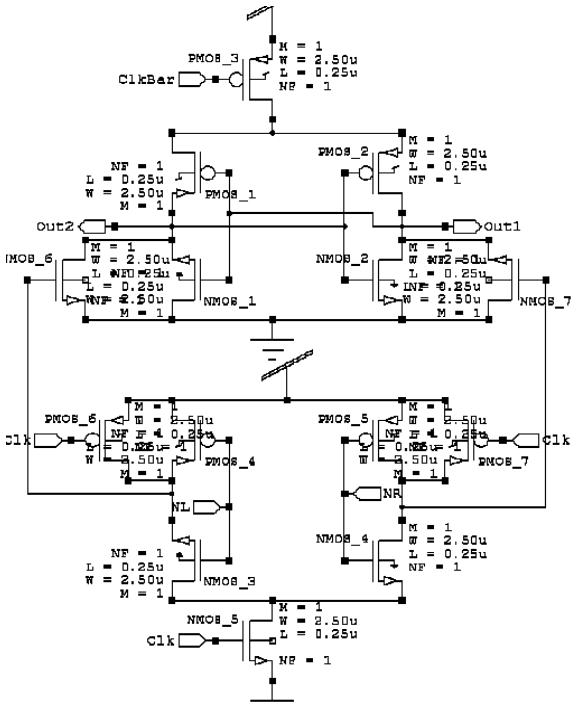


Fig.6 Circuit diagram Inverter based Differential Amplifier

The inverter-based amplifier topology shown in Figure 6 uses CMOS inverters as the amplifier input. This input stage design has the advantage of combining the transconductance of the n and p transistors. This combination of the two transconductance should provide 6dB increase in gain over a traditional common source amplification stage, with approximately the same DC bias current. When this architecture is implemented with a standard supply voltage ( $>2v_t$ ), the overall transconductance can be increased significantly depending on how transistors in the inverters are sized and the resulting current through the inverter. High current through the inverter allows significantly high bandwidths to be achieved. Another advantage of this topology is an increase in output swing and linearity when compared to a traditional common source or cascade amplifier if then respective trans conductance of the p and n type transistors are approximately equal in magnitude. For noise, the inverter-based topology offers lower equivalent noise resistance compared to the equivalent common source topology. When reset phase, CLK=0, PMOS3 & NMOS5 are off condition, PMOS6& PMOS7 are on condition. During this time, out1 and out2 discharging to VDD. When comparison phase

CLK=VDD, Tail transistors nmos5 and pmos3 are on state PMOS6 and PMOS7 are off condition. Input NL and NR is applied to the inverter, the inverter output continuously starts discharging according to the input provided.

### 3.1. Need of Low Voltage Circuits:

1. As the device channel length is scaled down into sub microns and the gate oxide thickness becomes only several nanometer thick, the supply voltage has to be reduced in order to ensure device reliability. With deep submicron processes now available, the maximum allowable supply voltage is decreasing from 5V to 3V and even to 2V.

2. The increasing density of the components on chip dictates low power. A silicon chip can only dissipate a limited amount of power per unit area. Since the increasing density of components allows more electronic functions per unit area, the power per electronic function has to be lowered in order to prevent overheating

3. Portable, battery-powered equipment needs low power to ensure an acceptable operation period from a battery, and the supply voltage must be as low as possible to reduce the number of batteries used. The main purpose of the input stage in Op Amp is to amplify differential signals and reject common-mode input voltages. An important specification of an input stage is the common mode input range. If the common mode voltage is kept within this range, the input stage will properly respond to small differential signals. Hence an application has to be designed such that the common mode input voltage stays within the common-mode input range.

### 3.2. APPLICATIONS OF COMPARATORS:

- Low power circuits
- Sensor interfacing
- ADC Flash Circuits
- ALU operations

### 4. OUTPUT SCREENSHOTS:

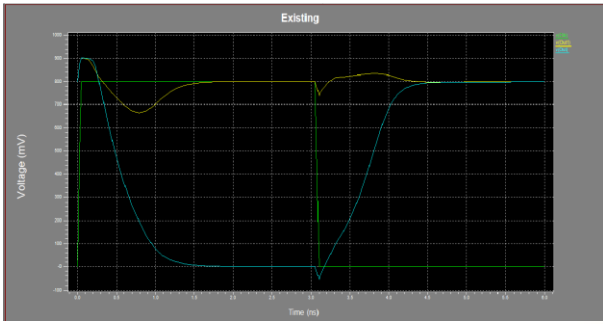


Fig7.Waveforms of Conventional dynamic comparator

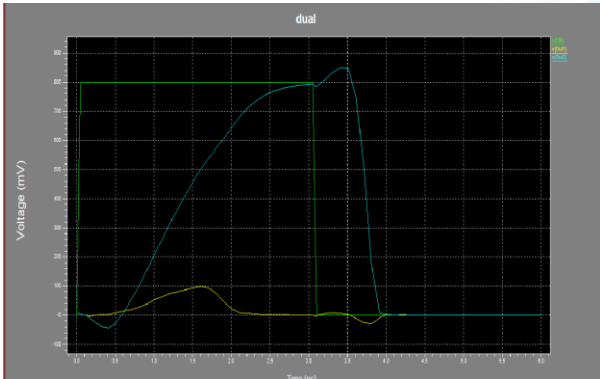


Fig 8.Waveform of Double Tail Comparator

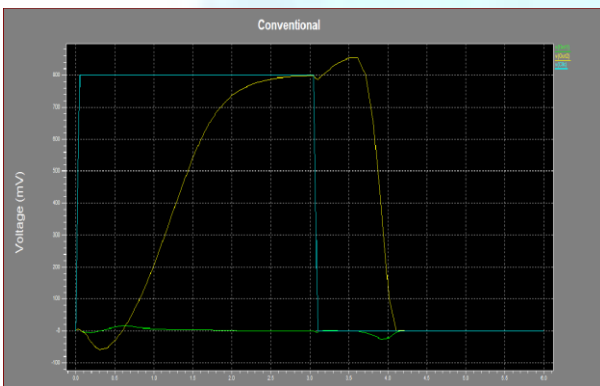


Fig 9.Waveforms of Double tail comparator with controlled transistors

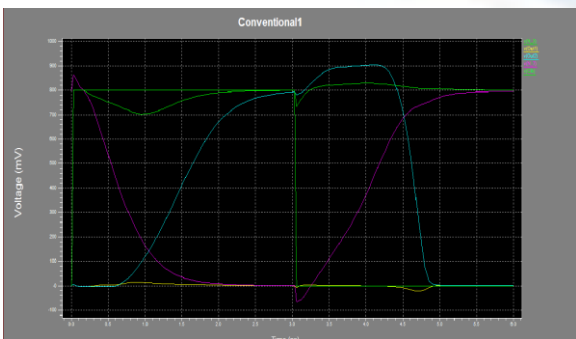


Fig 10.Waveforms of Double tail comparator with switched transistors

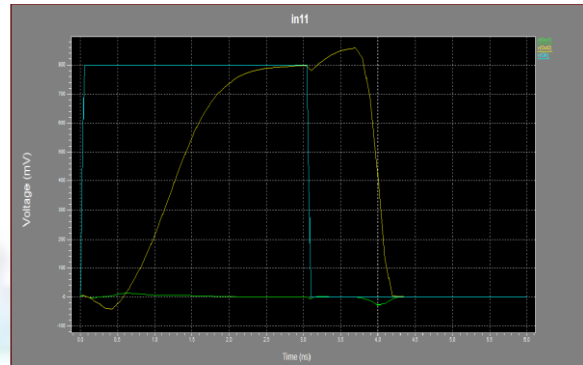


Fig 11.Waveforms of Inverter based Differential Comparator

### 4.1. SIMULATION RESULTS

Table 1.Simulation Results

Circuit	Power	Delay
Conventional Dynamic Comparator	3.158480e-008 watts	1.56E-09
Double Tail Comparator	7.982402e-008 watts	1.05E-11
Comparator with Controlled transistors	7.194841e-008 watts	9.89E-12
Comparator with Switched transistors	8.229026e-008 watts	2.92E-09
Inverter Based Differential Amplifier	7.446347e-008 watts	9.34E-12

### 5. CONCLUSION

In this paper, a comprehensive delay analysis for various comparators is done. Two common structures of conventional double tail comparator, Conventional dynamic comparators and Inverter based differential amplifier were analyzed. Analysis on delay, rise time, fall time, average delay time were done. A new inverter based differential amplifier with low-voltage low-power capability was proposed in order to improve the performance of the comparator. Simulation results in TSMC 0.18nm CMOS technology confirmed that the delay and power of the proposed comparator is reduced to a great extent in comparison with the conventional dynamic comparator and double-tail comparator.

## REFERENCES

- [1] B. Goll and H. Zimmermann, "A comparator with reduced delay time in 65-nm CMOS for supply voltages down to 0.65," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 56, no. 11, pp. 810–814, Nov. 2009.
- [2] S. U. Ay, "A sub-1 volt 10-bit supply boosted SAR ADC design in standard CMOS," *Int. J. Analog Integer. Circuits Signal Process*, vol. 66, no. 2, pp. 213–221, Feb. 2011.
- [3] A. Mesgarani, M. N. Alam, F. Z. Nelson, and S. U. Ay, "Supply boosting technique for designing very low-voltage mixed-signal circuits in standard CMOS," in *Proc. IEEE Int. Midwest Symp. Circuits Syst. Dig. Tech. Papers*, Aug. 2010, pp. 893–896.
- [4] B. J. Blalock, "Body-driving as a Low-Voltage Analog Design Technique for CMOS technology," in *Proc. IEEE Southwest Symp. Mixed-Signal Design*, Feb. 2000, pp. 113–118.
- [5] M. Maymandi-Nejad and M. Sachdev, "1-bit quantiser with rail to rail input range for sub-1V  $\Sigma\Delta$  modulators," *IEEE Electron. Lett.*, vol. 39, no. 12, pp. 894–895, Jan. 2003.
- [6] Y. Okaniwa, H. Tamura, M. Kibune, D. Yamazaki, T.-S. Cheung, J. Ogawa, N. Tzartzanis, W. W. Walker, and T. Kuroda, "A 40Gb/s CMOS clocked comparator with bandwidth modulation technique," *IEEE J. Solid-State Circuits*, vol. 40, no. 8, pp. 1680–1687, Aug. 2005.
- [7] B. Goll and H. Zimmermann, "A 0.12  $\mu\text{m}$  CMOS comparator requiring 0.5V at 600MHz and 1.5V at 6 GHz," in *Proc. IEEE Int. Solid-State Circuits Conf., Dig. Tech. Papers*, Feb. 2007, pp. 316–317.
- [8] B. Goll and H. Zimmermann, "A 65nm CMOS comparator with modified latch to achieve 7GHz/1.3mW at 1.2V and 700MHz/47 $\mu\text{W}$  at 0.6V," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2009, pp. 328–329.
- [9] B. Goll and H. Zimmermann, "Low-power 600MHz comparator for 0.5 V supply voltage in 0.12  $\mu\text{m}$  CMOS," *IEEE Electron. Lett.*, vol. 43, no. 7, pp. 388–390, Mar. 2007.
- [10] D. Shinkel, E. Mensink, E. Klumperink, E. van Tuijl, and B. Nauta, "A double-tail latch-type voltage sense amplifier with 18ps Setup Hold time," in *Proc. IEEE Int. Solid-State Circuits Conf., Dig. Tech. Papers*, Feb. 2007, pp. 314–315.