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Design and implementation of carry select adder for 128 bit low power

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Abstract:- Carry Select Adder is a prompt adder that is employed in processing of data processors for functioning quick arithmetic functions. Carry Select Adder (CSLA) is one of the fastest adders used in many data-processing processors to perform fast arithmetic functions. From the structure of the CSLA, the scope is to reduce the area of CSLA based on the efficient gate-level modification. In this paper 128 bit Regular Linear CSLA, Modified Linear CSLA, Regular Square-root CSLA (SQRT CSLA) and Modified SQRT CSLA architectures have been developed. To decrease area with insignificant speed penalty, set up a multiplexer basis add one circuit was projected. Based on this modification a new modified 32-Bit Square-root CSLA (SQRT CSLA) architecture has been developed. The modified architecture has been developed using Common Boolean Logic (CBL). The area of proposed design illustrates a decrease in support of 128-bit sizes which indicates attainment of method and not an easy trade-off of obstruction for area.

Keywords –Area efficient, Square-root CSLA (SQRT CSLA), Common Boolean Logic (CBL), Binary to Excess-1 CONVERTER (BEC).

1. INTRODUCTION

Design of area- and power-efficient high-speed data path logic systems are one of the most substantial areas of research in VLSI system design. In digital adders, the speed of addition is limited by the time required to propagate a carry through the adder. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position has been summed and a carry propagated into the next position. The CSLA is used in many computational systems to alleviate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum. In scheming of Integrated circuits, area occupancy plays an essential conscientiousness since intensifying requirement of portable systems. Speed of adding in digital adders, is restricted by time which is necessary to transmit a carry all the way through adder. The sum in elementary adder for each bit arrangement is produced successively subsequent to preceding bit position was summed and a carry transmitted into subsequent position [1].The basic idea of this work is to use Binary to Excess-1 Converter (BEC) sharing common Boolean logic term (CBL) instead of RCA with Cin=1 in the SQRT CSLA to achieve lower area and power consumption. The main advantage of this BEC logic comes from the lesser number of logic gates than the n-bit Full Adder (FA) structure. The difficulty of carry propagation delay is overcome by autonomously generating multiple radix carries and by means of this carries to choose among concurrently generated sums was put forward by Bedriji. A system was introduced by Akhilash Tyagi to make carry bits by block carry in 1 from carries of a block with block carry in 0. Carry Select Adder is a prompt adder that is employed in processing of data processors for functioning quick arithmetic functions.

To improve the intricacy of carry propagation delay carry select adder system is used in numerous computational systems by autonomously making numerous carries and subsequently selects a carry to produce the sum. By autonomously producing

multiple radix carries as well as usage of carries to select among concurrently generated sums, the difficulty of carry propagation impediment is prevailed over [3].128-bit Modified square-root carry select adder scheme have condensed area when compared with Regular Linear carry select adder system, Regular SQRT carry select adder system[2] in addition to Modified Linear carry select adder system.128-bit proposed modified SQRT CSLA is condensed when assessed with area of earlier CSLAs. The area of proposed design illustrates a decrease in support of 128-bit sizes which indicates attainment of method and not an easy tradeoff of obstruction for area.

2. METHODOLOGY:

Low power along with area efficient addition and multiplication has constantly been a basic requisite concerning high performance processors along with systems. Due to enhancement in portability of devices such as mobile, laptop and so on necessitates additional battery backup. In applications concerning electronics adders are mainly used. To alleviate the difficulty of carry propagation delay carry select adder system is used in numerous computational systems by autonomously making numerous carries and subsequently selects a carry to produce the sum [4].

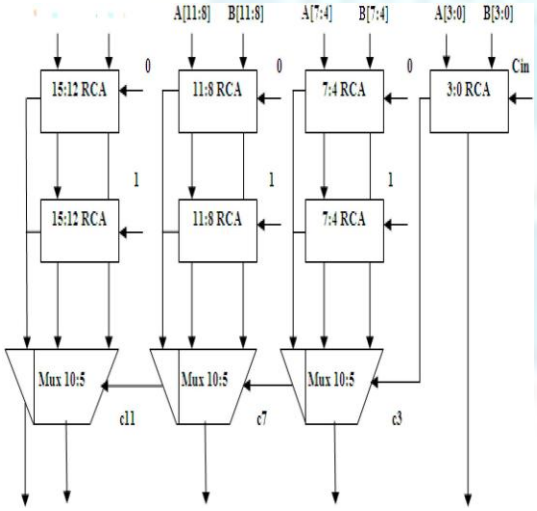


Fig. 1: Regular 128-bit Linear CSLA

The essential proposal is to exploit Binary to Excess-1 converter (BEC) to a certain extent than ripple carry adders[13] with carry in 1 in system of normal Carry select adder to achieve substandard area. The modified linear carry select adder system plus modified square-root carry select adder system provide improved outcomes when compared to regular system of linear carry select adder as well as regular square-root carry select adder. To decrease area with insignificant speed penalty, set up multiplexer basis add one circuit was proposed [5]. Based on a novel first zero detection logic, an area efficient Square-root CSLA system was introduced.

CSLA is practised for dropping area by single RCA in addition to an add one circuit as contrasting to using dual RCA[12]. By chaining number of equivalent length adder stages the linear carry select adder is build [6]. Equal size of inputs is specific to every block of adder and the steps leading towards assessment are specified. The fundamental square-root Carry Select adder include a dual ripple carry adder by 2:1 multiplexer, the most important complexity of regular carry select adder system is enormous area due to numerous pairs relating to ripple carry adder. The construction of 128-bit modified Square-root CSLA encloses different size RCA as well as BEC[12]. Linear CSLA includes analogous size ripple carry adders [7]. Each group holds dual ripple carry adders as well as multiplexer and achieves adding up by accumulation of small portions of bits and remains for carry to complete computation.

The structure of 128-bit regular Square-root CSLA comprises dissimilar size ripple carry adders and every group hold dual ripple carry adders as well as multiplexer. The time stoppage of linear adder[14] can decrease all the way through containing one more input into each set of adders than in previous set and is identified as Square-root CSLA.

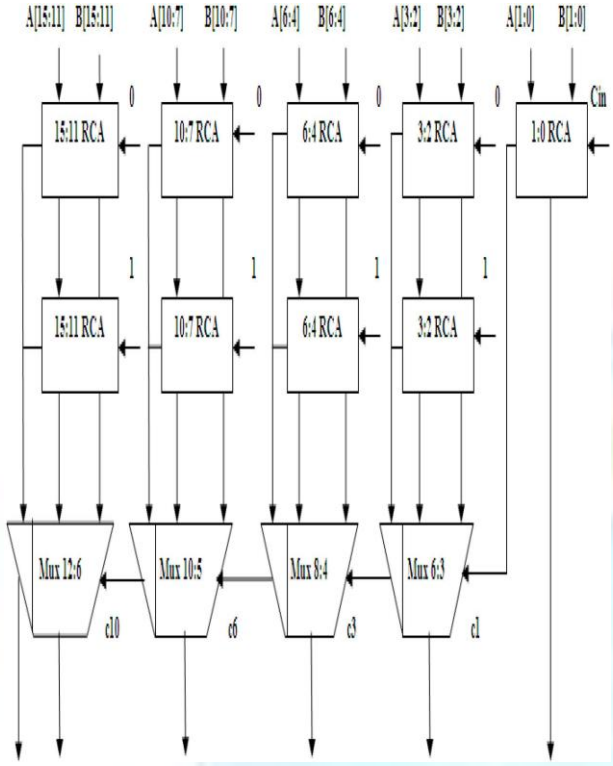


Fig. 2: Regular 128-bit SQRT CSLA

3. PROPOSED WORK

The main idea of this work is to use BEC instead of the RCA with Cin=1 in order to reduce the delay and area utilization of the regular SQRT CSLA. To replace the n-bit RCA, a n+1 bit BEC is required [8] this structure one input of the 8:4 mux gets as it input (B3, B2, B1, and B0) and another input of the mux is the BEC output. This produces the two possible partial outputs in parallel according to the control signal Cin. The importance of the BEC logic stems from the large silicon area reduction when the CSLA with large number of bits are designed. The modified 128-bit SQRT CSLA using BEC is shown in Fig.3. The structure is again divided into five groups with different sizes of Ripple carry adder and BEC. The group2, group3, group4 and group5 of 16-bit SQRT CSLA are shown in Fig.2. The parallel Ripple carry adder with Cin=1 is replaced with BEC. One input to the multiplexer goes from the RCA with Cin=0 and other input from BEC. Comparing the individual groups of both regular and modified SQRT CSLA, it is clear that the BEC[11] structure reduces delay. But the disadvantage of BEC method is that the area is increasing than the regular SQRT CSLA[15].

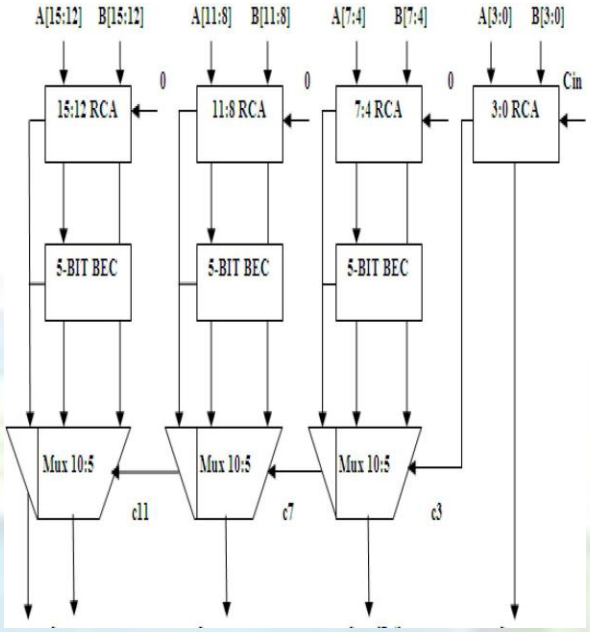


Fig 3: Modified 128-bit Linear CSLA

This method replaces the BEC add one circuit by Common Boolean Logic. The proposed 128-bit SQRT CSLA architecture is shown in Fig.3. The summation and carry signal for full adder which has Cin=1, generate by INV and OR gate. Through the multiplexer[9], the correct output result is selected according to the logic state of carry-in signal. The internal structure of the group3 of proposed CSLA is shown in Fig.4.

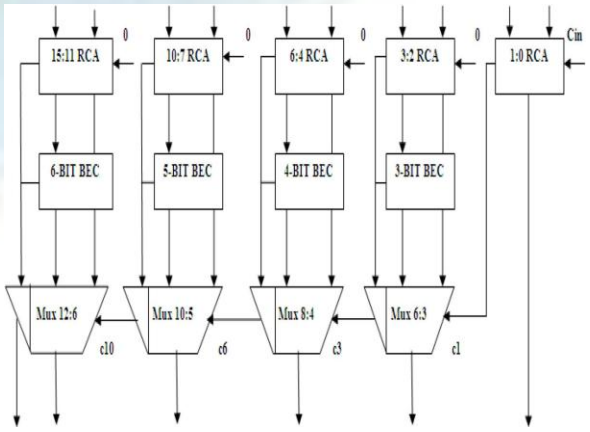


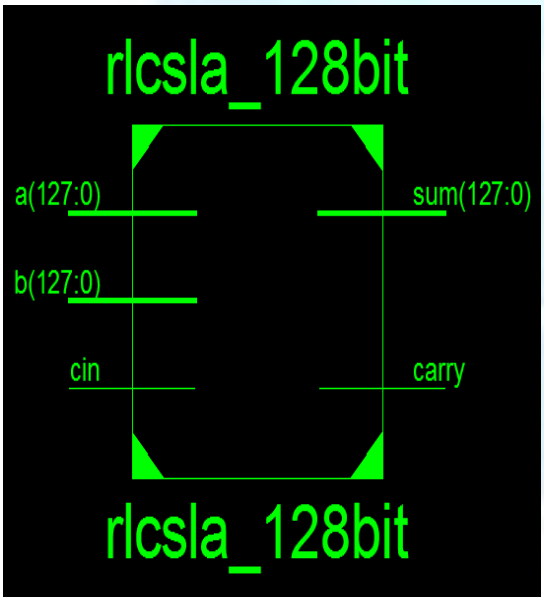
Fig.4: Modified 128-bit SQRT CSLA

4. FPGA IMPLEMENTATION AND RESULTS:

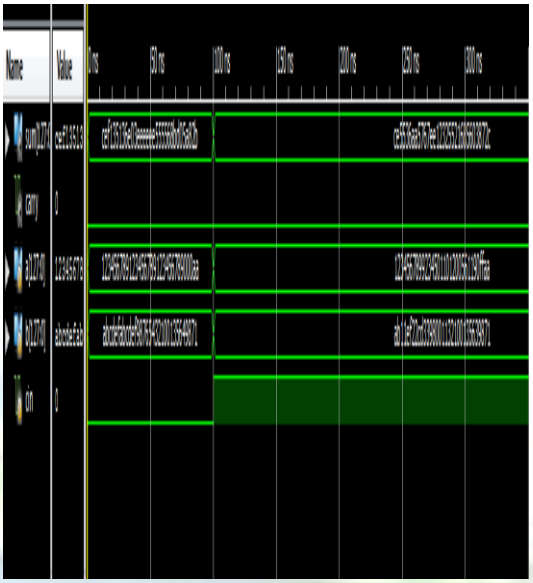
The modified linear carry select adder system plus modified square-root carry select adder system provide improved outcomes when compared to regular linear system of carry select adder along with regular system of square-root carry select adder. The Modified CSLA[10] construction is subsequently, low area, unsophisticated and efficient in support of VLSI hardware performance. The condensed numbers of gates recommend enormous advantages in reduction of area. 128-bit Modified square root carry select adder scheme have condensed area when compared with Regular Linear carry select adder system, Regular SQRT carry select adder system inaddition to Modified Linear carry select adder system. 128-bit proposed modified SQRT CSLA is condensed when assessed with area of earlier CSLAs.

Regular 128-bit Linear CSLA

Regular 128-bit Linear CSLA RTL SCHEMATIC

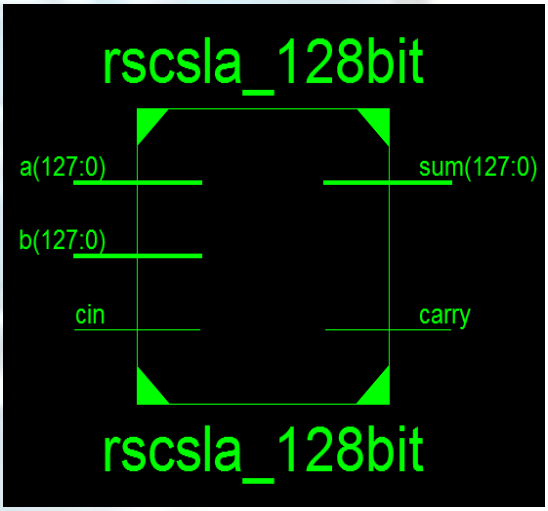


Regular 128-bit Linear CSLA OUTPUT WAVE FORM RESULT

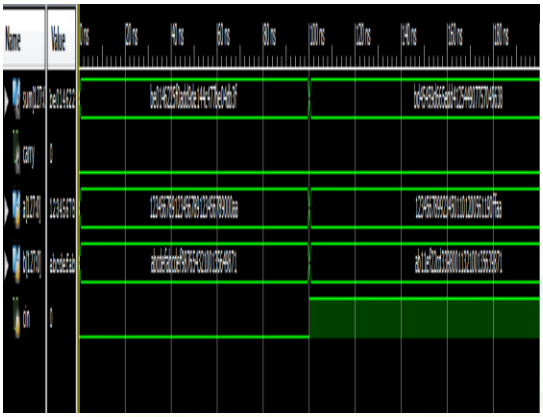


Regular 128-bit SQRT CSLA

Regular 128-bit SQRT CSLA RTL SCHEMATIC

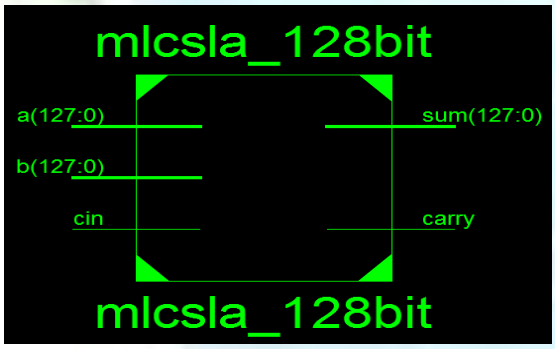


Regular 128-bit SQRT CSLA OUTPUT WAVE FORM RESULT

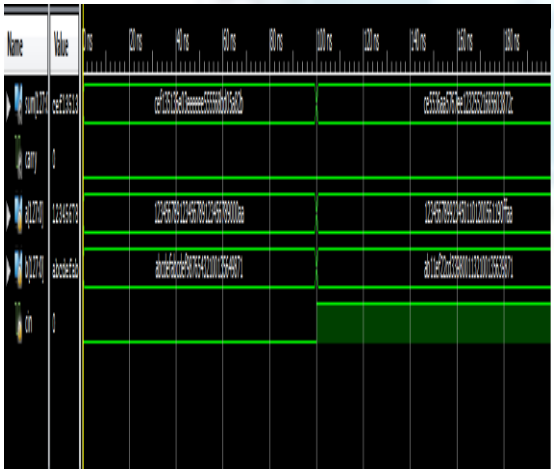


Modified 128-bit Linear CSLA

Modified 128-bit Linear CSLARTL SCHEMATIC

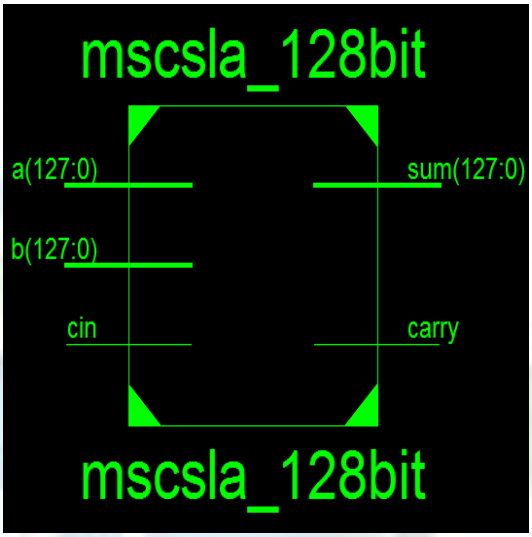


Modified 128-bit Linear CSLAOUTPUT WAVE FORM RESULT



Modified 128-bit SQRT CSLA

Modified 128-bit SQRT CSLARTL SCHEMATIC



Modified 128-bit SQRT CSLA OUTPUT WAVE FORM RESULT

5. CONCLUSION

SQRT CSLA are significantly reduced, proposed design show a decrease for 16-b, 32-b sizes which indicates the success of the method and reduced delay ,power and area. Carry Select Adder is a prompt adder that is employed in processing of data processors for functioning quick arithmetic functions. The regular

SQRT CSLA has the disadvantage of occupying more chip area. The reduced number of gates of this work offers the great advantage in the reduction of area. This paper proposes a scheme which reduces the area than the regular and modified SQRT CSLA. It would be interesting to test the design of the 64 and 128 bit SQRT CSLA.

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