

DRAM based on Self Controllable Voltage Level Technique for Leakage Power in VLSI

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Abstract:- Today trend is circuit characterized by reliability, low power dissipation, low leakage current, low cost and there is required to reduce each of these. Increase of chip complexity is consistently higher for memory circuits. The salient features such as low power, reliable performance, circuit techniques for high speed such as using dynamic circuits, and low leakage current, most of these have get give a better advantage. Power must be added to the portable unit, even when power is available in non-portable applications, the issue of low-power design is becoming critical. Thus, it is evident that methodologies for the design of high-throughput, low-power digital systems are needed. Since there is no additional circuitry needed for power reduction in this circuit design technique, there is no additional circuitry needed for power reduction Here 3T DRAM is implementing with self controllable voltage level (svl) technique is for reducing leakage current in 0.12um technology. The simulation is done by using microwind 3.1 & dsch2 and gives the advantage of reducing the leakage current up to 57%.

Keywords – low leakage power, high performance, self controllable voltage level technique, low cost, low power.

1. INTRODUCTION

DRAM designers have opted for a multiplexed addressing scheme. In this model the lower and upper halves of the address words are presented sequentially on a single address bus. This approach reduces the number of package pin and has survived through the subsequent memory generation. DRAMS [1]are generally produced in higher volumes. Lowering the pin count reduces the cost and size at the expense of performance. The presence of new address word is asserted by raising a number of strobe signals. Raising the row access strobe signal assert the MSB part of the address is present on the address bus, and that word decoding process can be initiated. The LSB part of the address is applied next and the column access strobe signal is asserted. Still leakage current may cause some power consumption even in the sleep mode. If the circuit could be designed such that there is very low leakage current in this mode, then the lifetime of the portable application will increase dramatically. The area efficiency of the memory array, i.e., the number of

stored data bits per unit area, is one of the key design criteria that determine the overall storage capacity and, hence, the memory cost per bit. Another important issue is the memory access time, i.e., the time required to store and/or retrieve a particular data bit in the memory array. The access time determines the memory speed, which is an important performance criterion of the memory array. Finally, the static and dynamic power consumption of the memory array is a significant factor to be considered in the design, because of the increasing importance of low-power applications. In the following, we will investigate different types of MOS memory arrays and discuss in detail the issues of area, speed, and power consumption for each circuit type Read-write (R/W) memory circuits, on the other hand, must permit the modification (writing) of data bits stored in the memory array, as well as their retrieval (reading) on demand. This requires that the data storage function be volatile, i.e., the stored data are lost when the power supply voltage is turned off. The read-write memory

circuit is commonly called Dynamic Random Access Memory (RAM), mostly due to historical reasons.

Dynamic random access memory (DRAM) is the most common kind of random access memory (RAM) for personal computers and workstations. The network of electrically-charged points in which a computer stores quickly accessible data in the form of 0's and 1's is called memory. Random access means that the PC processor can access any part of the memory directly rather than having to proceed sequentially from some starting place. DRAM is dynamic in that, unlike static RAM (SRAM), it needs to have its storage cells refreshed or given a new electronic charge every few milliseconds. that DRAM is much cheaper per storage cell and because each storage cell is very simple, DRAM has much greater capacity per unit of surface than SRAM. In the implementation of 3T DRAM using three NMOS M1, M2 and M3. M1 and M3 are the access transistor and by using these control the read and write operation. If the write operation is performed in that time M1 is on and M3 is off. The data is stored by charging the capacitor. If the read operation is performed in that time M1 is off and M3 is on, then the data is also available in that time also. When the 3T DRAM is implementing with Self-controllable Voltage Level technique one inverter is used in the upper part and the lower part. If we add this inverter in the circuit then the leakage power is less as compared to conventional 3T DRAM.. By using microwind 3.1 software, layout diagram have done. In this the word and VDD lines are implemented in poly, the connection to the MOSFETs occurs when poly runs over the active n+ area.

2.RELATED WORK

The paper shows a method based on a Capacitance discharge depth is planned [2]. The papers have constructed a measurement system which can make automatic remote monitoring of leakage current data using the Internet [2]. Method to approximation the difference of leakage current due to both intra-die and interdie gate length development changeability . Most of the works in leakage current analysis and reduction have stressed in a combinatorial circuits and sequential circuit. Memory circuits need more attention to design if leakage current is there. Various gate leakage reduction methodologies have been described in the literature such W. K. Luk et. al. gives a A Novel

Dynamic Memory Cell With Internal Voltage Gain. H. J. Yoo et. al. have developed A low voltage high speed self-timed CMOS logic for the multi-gigabit synchronous DRAM application[4]. JOHN E. et al give the idea of dram Design Using the Taper- Isolated Dynamic RAM Cell [3]. G. W. Taylor et al have developed A punch-through isolated RAM cell [5] .the idea about Leakage Model Including Source- Drain Partition shown in . Power Dissipation Analysis and Optimization for Deep Submicron CMOS Digital Circuits shown in .

The basic Fundamentals of Modern VLSI Devices and Principles of CMOS VLSI Design have developed. The device design guidelines for floating channel type surrounding gate transistor (FC-SGT) DRAM cells with high soft-error immunity described in this. The three structure studied, only SSMSL is a viable for the 0.6pm -pitch isolation of 256Mbit DRAM . Two leakage control transistors (a ptype and a n-type) within the logic gate for which the gate terminal of each leakage control transistor (LCT) is controlled by the source of the other shown in .

Transient effects of the floating body must be considered when designing for long data retention time. The use of the minimum idle time parameter, as a metric for evaluating different leakage control mechanisms, is shown. The experimental and simulation data of GIDL current as a function of 0.35- μm CMOS technology parameters and layout of CMOS standard cells is shown. The CMOS leakage current at the process level can be decreased by some implement on deep sub micron method shown .

3.PROPOSED WORK

As the trend for high-density DRAM arrays forces the memory cell size to shrink, alternative data storage concepts must be considered to accommodate these demands. In a dynamic RAM cell, binary data is stored simply as charge in a capacitor, where the presence or absence of stored charge determines the value of the stored bit. The data stored as charge in a capacitor cannot be retained indefinitely, because the leakage currents eventually remove or modify the stored charge. Thus, all dynamic memory cells require a periodic refreshing of the stored data, so that unwanted modifications due to leakage are prevented before they occur. The use of a capacitor as the primary storage

device generally enables the DRAM cell to be realized on a much smaller silicon area compared to the typical SRAM cell. Notice that even as the binary data is stored as charge in a capacitor, the DRAM cell must have access devices, or switches, which can be activated externally for "read" and "write" operations.

Dynamic random access memory (DRAM) is a type of random-access memory that stores each bit of data in a separate capacitor within an integrated circuit[6]. The capacitor can be either charged or discharged; these two states are taken to represent the two values of a bit, conventionally called „0's and „1's. Since capacitors leak charge, the information eventually fades unless the capacitor charge is refreshed periodically. Because of this refresh requirement, it is a dynamic memory as opposed to SRAM and other static memory. The main memory (the "RAM") in personal computers is dynamic RAM (DRAM). It is also used in the laptop and workstation computers as well as video game.

But this requirement does not significantly affect the area advantage over the SRAM cell, since the cell access circuitry is usually very simple. Also, no static power is dissipated for storing charge on the capacitance. Consequently, dynamic RAM arrays can achieve higher integration densities than SRAM arrays[7]. Note that a DRAM array also requires additional peripheral circuitry for scheduling and performing the periodic data refresh operations. The hardware overhead of the refresh circuitry, however, does not overshadow the area advantages gained by the small cell size.

3.1 4T Dynamic memory cell

Figure 1 shows schematic of 4T DRAM in which the read and write operation is performed when M3 and M4 ON. If M3 and M4 off, read and write operation is not performed.

The steady-state voltage: $V_{Cc} = V_{DD} - V_T$

- (i) Write "1" operation ($WL = 1$ - M3, M4 on) VC - forced to 0 by data write circuitry, V2 decreases to 0, M1 off; V1 increases; Final state: $V_1 = 1$, $V_2 = 0$
- (ii) Read "1" operation ($WL = 1$ - M3, M4 on) M1 off; M2, M4 on; VC - pulled down, $V_C > V_{Cc}$ read as a logic "1"
- (iii) Write "0" operation ($WL = 1$ - M3, M4 on) VC - forced to 0 by data write circuitry, V1 goes to 0, M2 off; V2 increases to 1 Final state: $V_1 = 0$, $V_2 = 1$

(iv) Read "0" operation ($WL = 1$ - M3, M4 on) M2 off; M1, M3 on; VC - pulled down, $V_C < V_{Cc}$ read as logic 0
The layout of 4T DRAM is shown in figure 1 in this diagram shows a NMOS is implemented by using a n+ diffusion layer and gate is implemented by using a polysilicon and interconnects are implemented by using metal1 and metal 2.

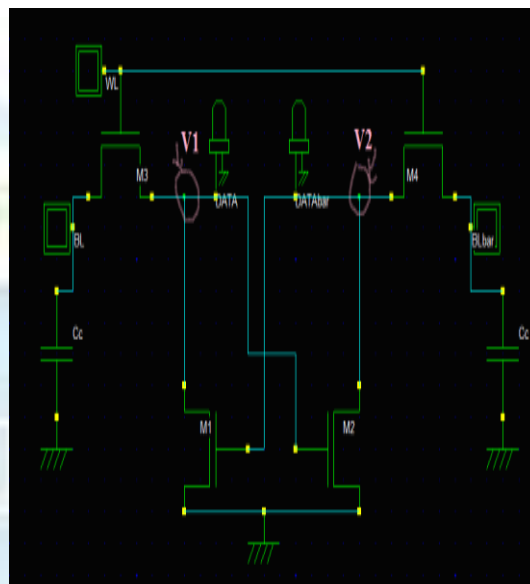


Fig 1 :shows schematic of 4T DRAM

The layout of 4T DRAM is shown in figure 2 in this diagram shows a NMOS is implemented by using a n+ diffusion layer and gate is implemented by using a polysilicon and interconnects are implemented by using metal1 and metal 2.

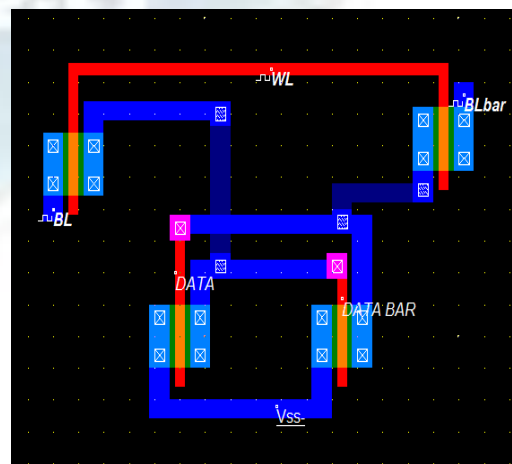


Fig2: shows a layout of 4T DRAM

Waveform of 4T DRAM is shown in figure 3. The read and write operation is shown. The read and write operation is activated when the word line is active in condition. If word line is not active condition circuit behaves as a open circuit .the leakage current in this time occur a 0.566ma and this is shown in diagram 4. the leakage current is the major factor to disturb the circuit behavior.

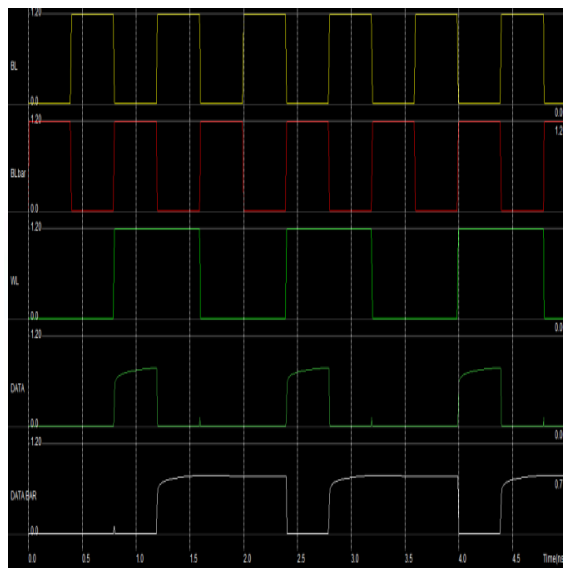


Fig 3: shows a waveform of 4T DRAM voltage versus time

4. Low Power Techniques

A) Supply Voltage Scaling

To reduce the power consumption, the scaling power supply voltage is most effective method [7]. Reducing the supply voltage can significantly reduce the power dissipation that is a quadratic function of the operating voltage.

B) Reducing Effective Capacitance

When the performance loss in throughput due to lowering the supply voltage is not acceptable. The low power consumption in CMOS circuits can also effective the reducing capacitance.

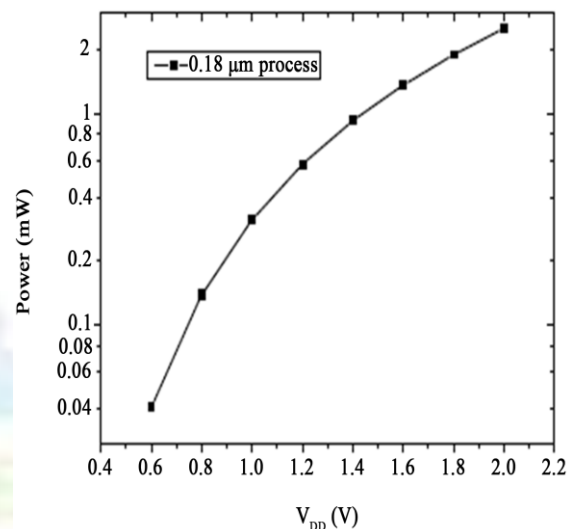


Fig 4: Power consumption for a 4-bit CLA as a function of Vdd

4.1. Effects of Circuit Styles

The different circuit and logic styles result in different gate and diffusion capacitance of the transistors in a combinational logic circuit [8]. Some of the circuit styles can substantially reduced the physical capacitance and is good for low-power operation. Figure 3 represents the power-delay products of an 8-bit adder relationship between that was implemented in 2 μ m CMOS technology with different circuit styles and the corresponding propagation delays. As shown in Figure 4, the adder that was implemented by using complementary pass transistor logic (CPL) is about twice as fast as the conventional static CMOS. This is due to that CPL improves the performance of the circuit with a lower input capacitance and reduced voltage swing. Moreover, a CPL logic circuit consumes less power than a static CMOS one, for instance, the power saving for a CPL adder is about 30% compared to a conventional static CMOS adder [9].

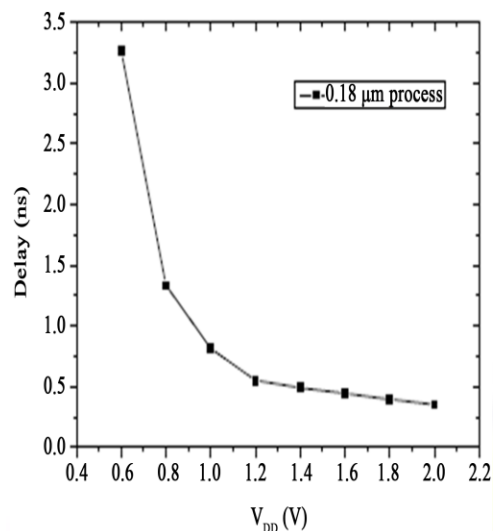


Fig 5: Propagation delay versus V_{DD} for a 4-bit CLA adder

4.2. Transistor Sizing

The capacitive load that originates from transistor capacitance and interconnect wiring can be reduced by optimizing transistor sizes whenever possible and reasonable.

In general, increasing the transistor sizes results in a large (dis)charging current and simultaneously increases the parasitic capacitance. On the other hand, reducing the transistor sizes will result in decreasing input capacitance that may be the load capacitance for other gates and lowering the speed of the circuit.

4.3. Minimizing Glitching Activity

Glitches, or dynamic hazards, are unwanted signal transitions which occur before the signal settles to its intended value. Glitches can be generated and propagated in both data path and control parts of the circuits.

5. THE SOURCES OF LEAKAGE CURRENT

There are three main sources of leakage current that the designer must minimize. They are the source/drain junction leakage current, the gate tunneling leakage and the sub-threshold leakage current through the channel of an OFF transistor. The source/drain junction leakage current from the drain and the source to the substrate is due to the fact that the junction acts like a

reversed biased diode when the transistor is off. The magnitude of this current depends on the size of the diffusion area of the transistor which depends on the process technology. The gate tunneling current flows through the gate oxide into the substrate and increases exponentially when the gate oxide becomes thinner. It also increases with the increase of supply voltage. It is important to control the high-K gate dielectric leakage current if the low power device is in sleep mode. The sub-threshold leakage current is a leakage current from drain to source. It is a diffusion current that is built up by minority carriers in the channel of the MOS device[10]. The MOS transistor is operating in a weak inversion mode (sub-threshold mode).

5.1 LEAKAGE POWER REDUCTION TECHNIQUES

Various leakage power reduction techniques have been proposed in the past. Won et al. [11] 2003 proposed an MTCMOS design methodology for mobile computing. Multi-threshold CMOS (MTCMOS) technology provides low leakage and high performance operation by using high speed, low V_t transistors for logic cells and low leakage, high V_t devices as sleep transistors as shown in Fig. 3. Commonly used processes are double (low and high) or triple (low, normal and high) multi threshold values. The sleep transistors are to disconnect the logic cells from the supply lines in order to reduce the leakage current in sleep mode. This is also referred to as power gating technique wherein circuit blocks that are not in use are temporarily turned off to reduce the overall leakage power. This temporary shutdown time can also called low power mode or inactive mode. When circuit blocks are required for operation, they are activated to active mode. These two modes are switched at the appropriate time in a suitable manner to maximize power performance while minimizing impact on performance. Thus goal of power gating is to minimize leakage power by temporarily cutting power off to selective blocks that are not required in that mode. The main concerns here are wake up latency and power plane integrity. If we suppose that there is a sleep/wake up signal provided from a power management unit, the wake up period of time can affect the overall performance of the circuit. Thus it is very important to minimize the time required to turn on the circuit upon receiving the wake up signal. A low threshold value transistor is very fast but it has quite large sub-threshold leakage currents. This sub

threshold leakage current will be a very important problem when a sleep-mode circuit is constructed. If the sleep-mode is to be effective, this static leakage current must be as small as possible. So if higher threshold value transistors are used to gate ground and also perhaps the powers supply (VDD)[15], the lower threshold value transistors are used to perform the circuit function. The higher threshold value transistors will then reduce the sub-threshold leakage current dramatically, but the circuit will then continue to have the same performance as before.

The MTCMOS [12] approach is easy on combinatorial circuits, but it can be tricky on sequential circuits. Should the power supply be turned off, all data stored in the circuit will be irreversibly lost. This is the main problem with MTCMOS circuits. This will also require a larger die area and impose higher power losses. CMOS (VTCMOS) devices are one solution to this problem. In VTCMOS technique[13], the threshold voltage of the low threshold devices is varied by applying variable substrate bias voltage from a control circuitry.

5.2 Lowering supply voltage:

Supply voltage scaling which has originally been developed for the reduction of switching power may be used to reduce leakage power since sub-threshold leakage and the leakage due to DIBL decrease when the supply voltage is lowered. This may be implemented in either a static fashion using multiple power supplies or in a dynamic one using a single power supply but lowering both the voltage and frequency when performance demand is low. This is equivalent to lowering the supply voltage as fast as the circuit goes into the sleep mode and it can be used for reducing the leakage power consumption of VLSI circuits[14].

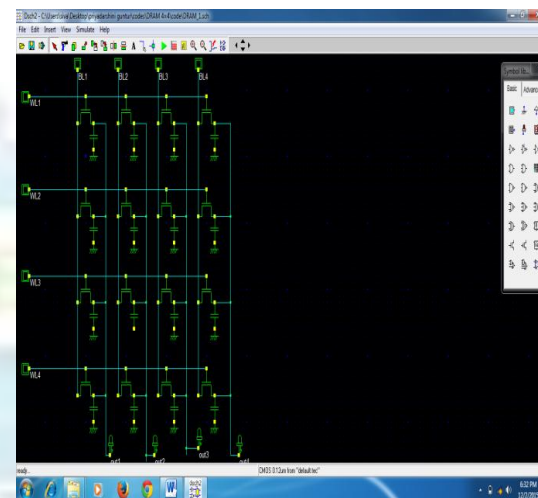
5.3 Leakage control by adding control pins:

This method of reducing the leakage current is similar to vector input control. However, in this method the inner states of the circuit are controlled. These signals can be controlled in two ways, either by multiplexing the signals or by modifying the gates. The multiplexing method is controlled by a sleep signal that is deciding the state of the multiplexer. When the sleep signal is off the circuit operates as normal and when the sleep signal is on a fixed value, it is set as input signal.

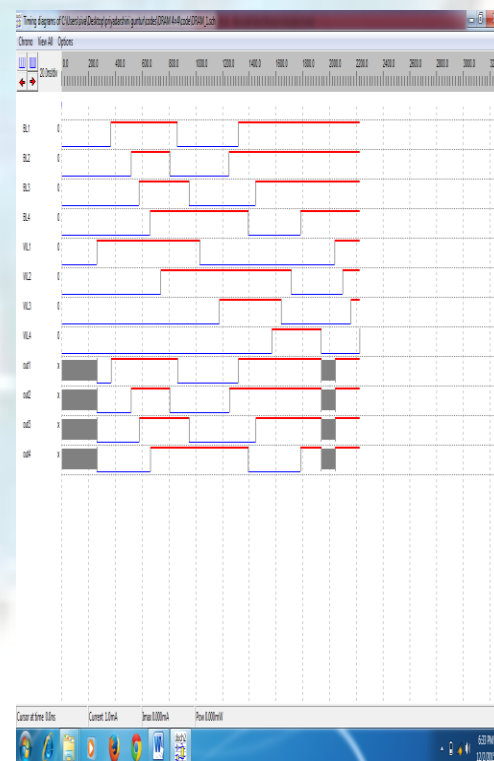
6.RESULTS:

DSCH

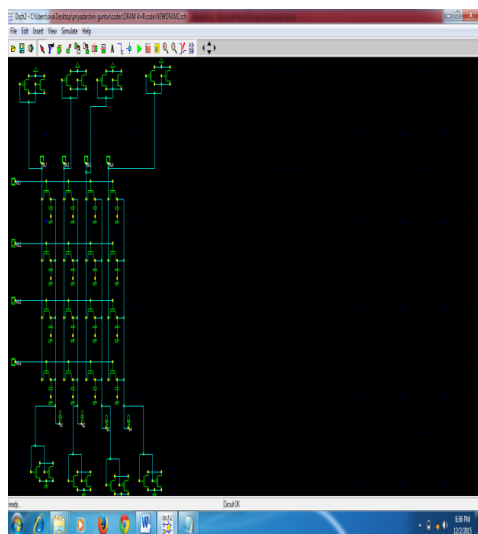
NORMAL DRAM 4X4



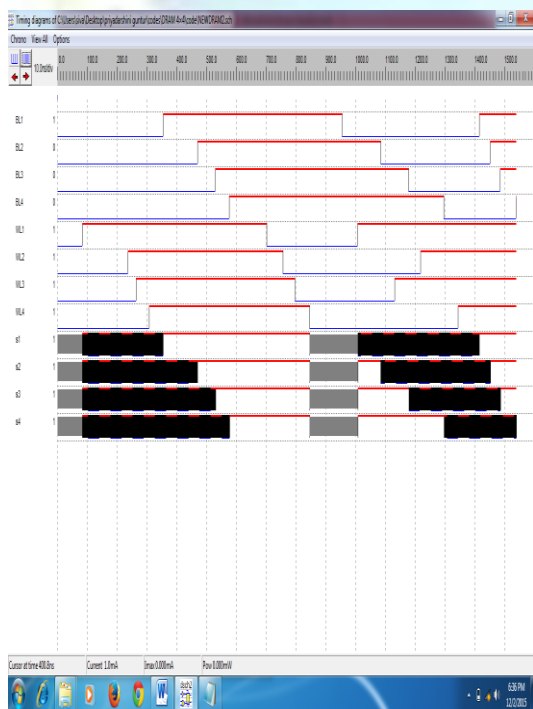
OUTPUT



SELF CONTROLLABLE DRAM 4X4

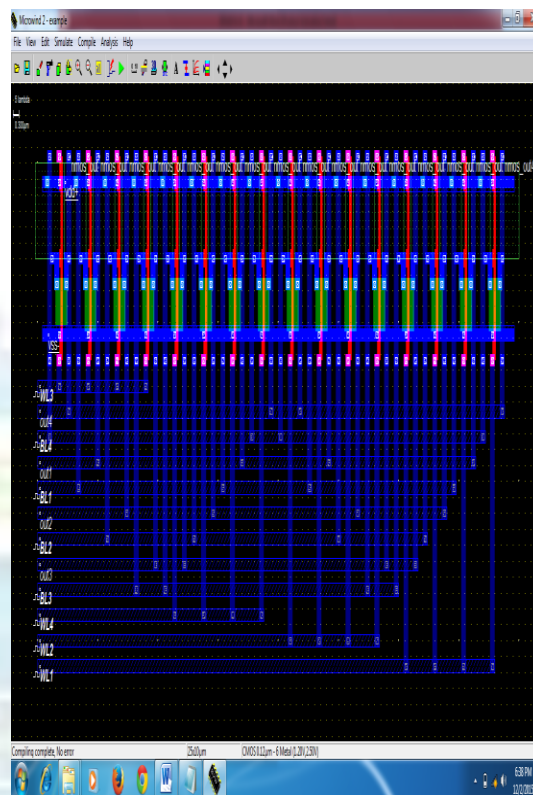


OUTPUT

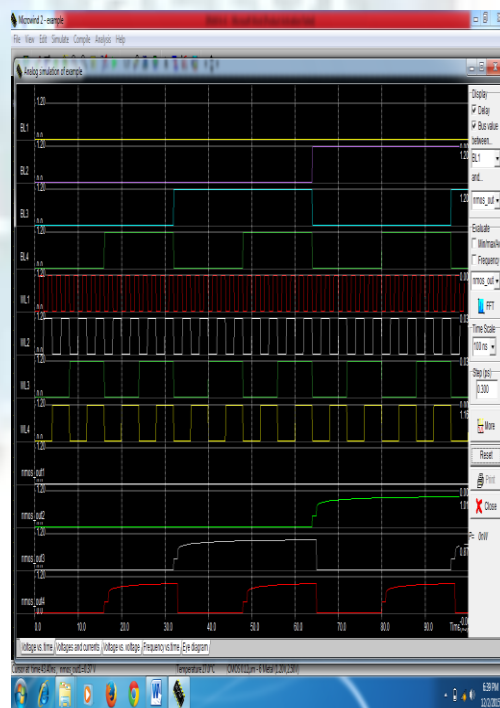


MICRO WIND

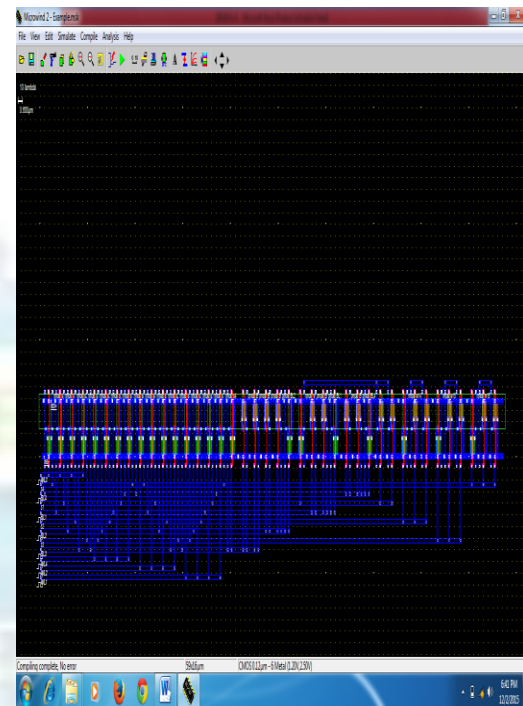
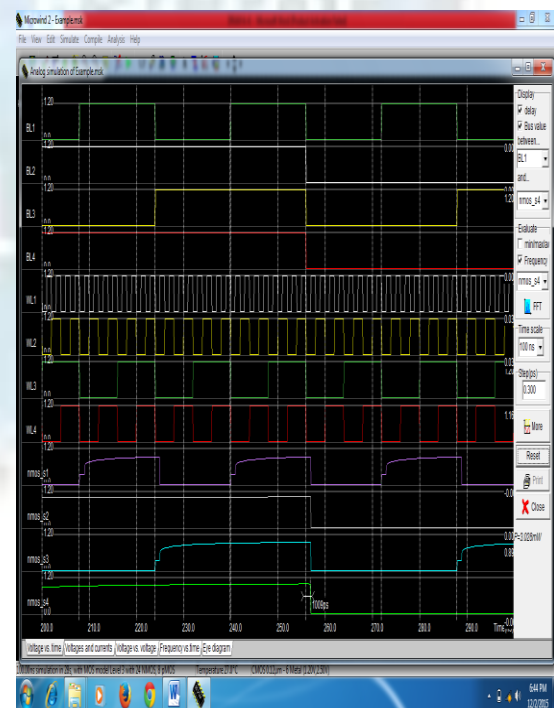
NORMAL DRAM 4X4



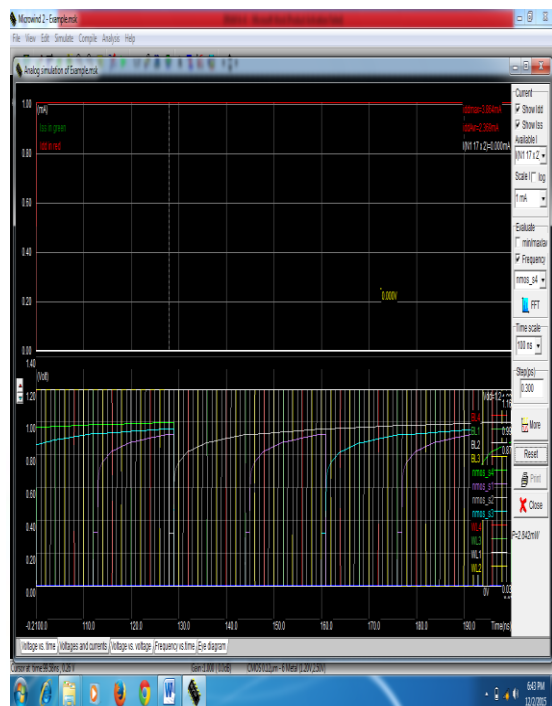
VOLTAGE VS VOLTAGE



The screenshot displays the Microcap 12 software interface. The main window shows two plots: a top plot for voltage (Vn) and a bottom plot for current (In). The top plot shows a step function with a voltage of 1.0V. The bottom plot shows a step function with a current of 1.0A. The right panel shows the simulation settings, including the time scale (100ns) and the simulation type (Transient). The bottom status bar shows the simulation time (100ns) and the simulation type (Transient).

[illegible]

VOLATGE AND CURRENTS



VLOTAGE VS VOLTAGE



CONCLUSION

4T DRAM with self controllable voltage level is implemented by using a microwind 3.1 and DSCH 2. it's a beneficial for reduction up to 67% of the leakage current. To reduce these improve the performance and speed of the design. The power supply (VDD) is used 1.2v. Here 90nm technology is used. To implement these technology power dissipation is also reduced. Its also improved further by change in width to length ratio. To implement 3T DRAM with self controllable voltage level gives the advantageous of reduction up to 57%.

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