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Performance Analysis of High Speed CMOS Full Adder Circuits For Embedded System

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Abstract---The full Adder is designed using CMOS logic style by dividing it in three modules so that it can be optimized at various levels. First module is an XOR-XNOR circuit, which generates full swing XOR and XNOR outputs simultaneously and have a good driving capability. The main motive is to determine the comparison of power, surface area and complexity of Full adder designs using CMOS Logic Styles. Logic style affects the switching capacitance, transition activity, short circuit current and delay. Various logic styles have been compared taking full adder as a reference circuit and power dissipation and delay as reference parameters. Full adder Design is better compared to conventional design. Transistor Design with respect to power, delay, Power Delay Product Comparison. It is observed that less power is consumed in the Transmission based full adder than the Convention full adder and Pass Transistor full adder.

Keywords--- CMOS logic style, full adder, high speed, low power.

1. INTRODUCTION

Full adder is a basic building block for various arithmetic circuits such as multipliers, compressors, comparators and so on. The power requirement and output delay of these circuits is greatly depending upon the power requirement and delay of the full adder circuits. In many computers and other kinds of processors, adders are used not only in the arithmetic logic unit(s), but also in other parts of the processor, where they are used to calculate addresses, table indices, and similar operations. So for designing the high performance arithmetic circuits, minimization of the power and delay of the full adder circuit is required. Although adders can be constructed for many numerical representations, such as binary-coded decimal or excess-3, the most common adders operate on binary numbers. Multipliers are the key elements in several Computer Arithmetic circuit applications like Image and video Processing, Multimedia like in Oscillators and Microprocessors like in ALUs, Multiplier and accumulator units, Digital Signal Processors like in Filter designing, convolutors etc.In most of the VLSI systems, multiplier lies in the critical path directly. The performance of multipliers helps in influencing the performance of several DSP algorithms and processor's running speed. Computational and market demands have driven VLSI microprocessors to double their performance every three years. A good circuit design and choice of appropriate logic style is equally important in achieving this performance goal. Power and area consumption are two important considerations for VLSI system designer engineers. The designers are now focusing on multipliers of high speed and at the same time maintaining low power consumption and further to have low power delay product.

Several logic styles for designing the Full adder have been proposed. In classical design of full adder normally single CMOS structure is used for the whole design, Such as the standard static CMOS full adder is based on regular CMOS structure with conventional pull-up and pull-down transistors providing full swing output and good driving capabilities but the main drawback of this circuit is high input capacitance and use of large no. of PMOS, due to which the speed of this structure is degraded. In another conventional design the complementary pass transistor logic (CPL) is used, which provides good driving capability, full swing of operation and high speed, but its main disadvantage is high power dissipation due to large number of internal nodes in the cell. Designing an Arithmetic Unit at a particular

circuit level effects its performance as various performance determining factors such as switching capacitance, transition activity and short circuit current are strongly influenced by chosen logic style. The speed of dynamic CMOS logic style adder is higher. It has several demerits such as charge sharing, high clock load, higher switching activities and lower noise immunity and it requires high power for driving the clock lines. Another logic styles are transmission-gate full adder (TGA) and transmission-function full adder (TFA) based upon transmission gates and transmission function theory. These full adders are very low power consuming, but have very low driving capabilities. In order to optimize the reduction phase, compressors can be used for partial product accumulation. Column Compression (CC) is the technique used to reduce the power consumption and delay in multiplier design, in which the compressors used in multipliers are accumulated with partial products column–wise.

"CMOS" refers to both a particular style of digital circuitry design, and the family of processes used to implement that circuitry on integrated circuits (chips). CMOS circuitry dissipates less power than logic families with resistive loads. CMOS logic design style uses more than one module for designing of full adder. In this design style full adder structure is designed by breaking the full adder into three modules. Module I is an XOR-XNOR circuit which drives the other modules, So it must have good driving capability and provide full swing outputs simultaneously. Module II and Module III are the sum and carry circuits which use the output of first module and third input signal as input to produce the sum and carry outputs respectively. General structure of hybrid CMOS design style is shown in Fig.1. General structure of hybrid CMOS design style is shown in fig.1. This logic design style provides the freedom to take the optimum circuits for every module for getting the optimum performance of adder cell. These adders generally lack the driving capabilities. Their performance as a single bit is good, but as the size of chain increases, the performance degraded drastically. But in this paper we tried to present an adder cell with this logic style for which the performance is not degraded in adder chain. We tried to get better delay performance from Cin to Cout and evaluate the performance of adder cell in 4 bit adder chain and 8 bit adder chain.

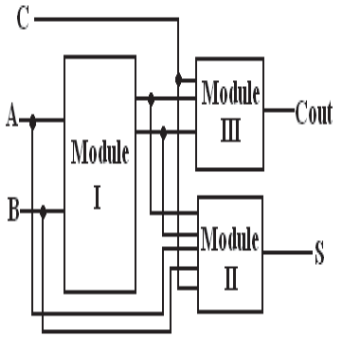

Fig.1. General Form of CMOS logic design

2. CMOS LOGIC DESIGN

Although substantially increasing design productivity, such tools require the employment of a long chain of automatic synpaper algorithms, from register transfer level (RTL) down to gate level and net list.

2.1 CMOS Technology:

Complementary metal–oxide–semiconductor (CMOS) is a technology for constructing integrated circuits. CMOS is also sometimes referred to as complementary-symmetry metal–oxide semiconductor (or COS-MOS). The words "complementary-symmetry" refer to the fact that the typical digital design style with CMOS uses complementary and symmetrical pairs of p-type and n-type metal oxide semiconductor field effect transistors (MOSFETs) for logic functions. CMOS technology is used in microprocessors, microcontrollers, static RAM, and other digital logic circuits. CMOS technology is also used for several analog circuits such as image sensors, data converters, and highly integrated transceivers for many types of communication.

Two important characteristics of CMOS devices are high noise immunity and low static power consumption. Significant power is only drawn when the transistors in the CMOS device are switching between on and off states. Consequently, CMOS devices do not produce as much waste heat as other forms of logic. CMOS also allows a high density of logic functions on a chip. It was primarily for this reason that CMOS became the most used technology to be implemented in VLSI chips. The phrase "metal–oxide–semiconductor" is a reference to the physical structure of certain field-effect transistors, having a metal gate electrode placed on top of an oxide insulator, which in turn is on top of a semiconductor.

C_{in}	A	B	SUM	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	0	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

The sum (S) and carry (Cout) expression for a 1-bit full adder with three binary inputs A, B and Cin are given by In CMOS architecture, we get XOR and XNOR of A and B inputs as the intermediate signal at the output of module I. These input signals and Cin are available for the input of module II and module III. So we get new expression for sum and carry using XOR output H and XNOR output H'. Static CMOS type of XOR-XNOR module uses both pMOS and nMOS transistors and it consumes large amount of power and many transistors and so larger area. Static XNOR-XOR also uses Complementary CMOS style of pull-up and pull-down transistors, but it also has large power consumption and not used at low voltages. To have high speed performance than the earlier three types of XOR-XNOR gates, it is convenient to use the XOR-XNOR module as shown in Fig.2. It can operate well at low supply voltages and it uses only 8 transistors

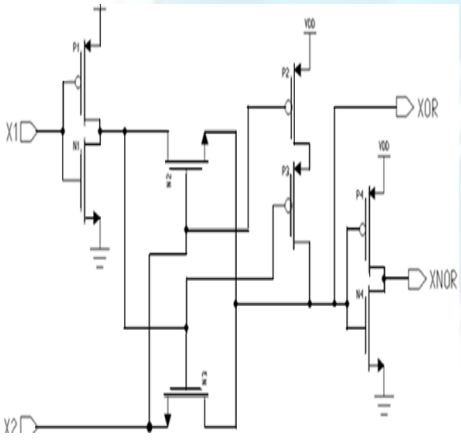

Fig.2. Circuit diagram of XOR-XNOR

2.2 CMOS Process Enhancements:

1) Silicon on Insulator:

As the name suggests transistors are fabricated on an insulator (SiO2 or sapphire) Insulating substrate eliminates capacitance between the source/drain and body, higher speed devices and low leakage currents.

2) Transistors:

Multiple threshold voltages and oxide thicknesses Processes offer multiple threshold voltages Low threshold devices: faster, higher leakage.

2.3 Design and Architecture of Full Adder:

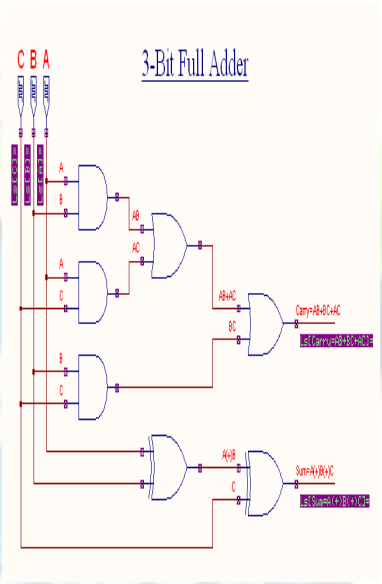

Fig.3. 3-.4bit full adder

Truth table adder designThe ultimate goal of a binary full-adder (BFA) is to implement the following truth table for each bit:
Logically, carry = AB+BC+CA and Sum = C⊕B⊕A, where k is an integer 0 to n for an n-bit adder. Generally, adders of n-bits are created by chaining together n of these 1-bit adder slices.

3. Existing System Design

Digital schematic is designed using DSCH for full adder using 28 transistors which occupies a lot of surface area and power consumed is also high which can be reduced by reducing number of transistors. The complexity can be decreased by modifying this existing full adder design.The twenty eight bit transistor based on regular CMOS structure i.e. pull-up and pull-down network. One of the most significant advantages of this full adder waists high noise margins and thus reliable operation at low voltages.

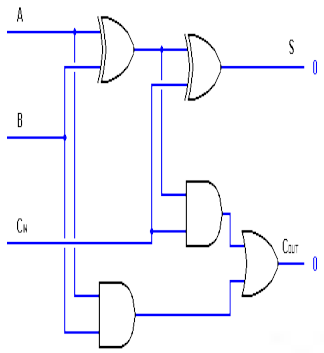

Fig.4. The gate level implementation for explanation of full adder

Here implementation of the full adder circuit is designed by taking the logic equations and translate them directly into complementary CMOS circuit in fig. . Some logic manipulations can help to reduce the transistor count. For instance, it is advantageous to share some logic between the sum and carry – generation sub circuits, as long as this does not slow down the carry generation, Which is the most critical part as stated previously. The following is an example of Such as reorganized equation set:

$$C_{out} = A.B + B.C_{in} + A.C_{in}$$

$$S = A.B.C_{in} + C_{out}\ (A + B + C_{in})$$

The equivalence with the original equations is easily verified. The corresponding adder design, using complementary static CMOS, is shown in figure and the gate level implementation is shown in figure. The transistors of the circuit produce the C_{out} and the remaining transistors produce the Sum outputs. Therefore the delay for computing C_{out} is added to the total propagation delay of the Sum output. The structure of this adder circuit is huge and thereby consumes large on-chip area.

4. POWER DISSIPATION

There are three sources of power dissipation viz. static power, dynamic power and short circuit power dissipation. Static power dissipation is associated with leakage current and can be improved with the advancement in fabrication technology only. Dynamic power dissipation is given by the following equation:

$$P_d = \alpha C_L V_{DD}^2 f_{CLK}$$

Where α is the switching activity, is the load capacitance, V_{DD} is the supply voltage and f_{CLK} is the clock frequency.

Other source of power dissipation is short circuit power dissipation that arises when direct current flows from V_{DD} to ground. Short circuit power dissipation, depends on rise time and fall time because it is only during transition that transistors between V_{DD} and ground remains on and short circuit power dissipation comes into play. In the optimized full adder circuit, both transistor count and area has been reduced that lowers the dynamic power dissipation as well as short circuit power dissipation and hence the total power dissipation reduces.

Circuit (Full Adder)	**Power**		
	180 nm	90 nm	45nm
CMOS Full Adder	3.998E-6	348.9E-9	79.12E-9
TG Full adder	1.519E-6	180.7E-9	24.86E-9
Pass Transistor Full Adder	1.823E-6	251.8E-9	27.36E-9

Comparison among various Adders

5. CONCLUSION

Using CMOS logic design style the designer can able to select the various modules in a circuit depending upon the application. Using the adder categorization and CMOS design style, many full adders can be designed. The circuit uses the XOR-XNOR gate which provides good driving capability, high speed and low power. The CMOS full adder has better performance than most of the standard full-adder cells owing to the novels design modules. Also it has been shown that reducing the supply voltage is the most direct means of reducing dissipated power and operating CMOS devices is considered to be the most energy-efficient solution for low-performance applications. It performs well with supply voltage ranging from 1.2V to 2.4V. When embedded in a parallel adder chain, it outperforms all the other adders making it suitable for larger arithmetic circuits. Hence reduced complexity is achieved by using less number of transistors. Also power is reduced up to

30% in comparison to conventional design.

6. REFERENCES

[1] N. Weste, and K. Eshranghian, "Principles of CMOS VLSI Design: A System Perspective," Reading MA: Wesley, 1993.

[2] Sanjeev Kumar and Manoj Kumar "4-2 Compressor design with New XOR-XNOR Module", 4th International Conference on Advanced Computing and Communication technologies, pp. 106-111, 2014.

[3] Meher, P.; Mahapatra, K.K. "Low power noise tolerant domino 1-bit full adder", International Conference on Advances in Energy Conversion Technologies (ICAECT), pp. 125 – 129, 2014

[4] Vojin G. Oklobdzija, "Simple and Efficient Circuit for Fast VLSI Adder Realization," IEEE International Symposium on Circuits and Systems Proceedings, 1988, pp. 1-4.

[5] J.Rabaey, "Digital Integrated Circuits: A Design Prospective," Prentice- Hall, Englewood Cliffs, NJ, 1996.

[6] R. Zimmermann and W. Fichtner, "Low-power logic styles: CMOS versus pass-transistor logic," IEEE Journal of Solid–State Circuits, vol.32, pp.1079-1090, July 1997.

[7] http://en.wikipedia.org/wiki/CMOS

[8] Devi, Padma, Ashima Girdher, and Balwinder Singh. "Improved carry select adder with reduced area and low power consumption." International Journal of Computer Applications 3.4 (2010): 14-18.

[9] D. Radhakrishnan, "Low-voltage low-power CMOS full adder," IEEE Proc. Circuits Devices Syst., vol. 148, no. 1, pp. 19–24, Feb. 2001.

[10] S.Veeramachaneni, M.B. Srinivas, "New improved 1-bit full adder cells", IEEE Conf. Electrical and computer engg. May2007.

[11] S. Goel, Ashok Kumar and M. A. Bayoumi, "Design of robust, energyefficient full adders for deep-sub micrometer design using Hybrid-CMOS logic style", IEEE Trans. Very Large Scale Intsgr. (VLSI) Syst., vol. 14, no. 12, Dec. 2006.

[12] M. Shams, T. K. Darwish, and M. A. Bayoumi, "Performance analysis of low-power 1-bit CMOS full adder cells," IEEE Transactions on VLSI Systems, vol. 10, pp. 20–29, Feb. 2002.

[13] Sohan Purohit, Martin Margala, Macro Lanuza and Pasquale Corsonello, "New Performance/Power/ Area Efficient, Reliable Full Adder Design", GLSVLSI'09, ACM May,2009.

[14] Kshirsagar, R.V. "Design of low power column bypass multiplier using FPGA", Electronics Computer Technology (ICECT), 2011 3rd International Conference on, On page(s): 431 - 435 Volume: 3, 8-10 April 2011

[15] Prabhu, A.S.; Elakya, V. "Design of modified low power booth multiplier", International Conference on Computing, Communication and Applications (ICCCA), pp. 1 - 6, 2012.

