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ASIC Design of Reversible Full Adder and Multiplier Circuits

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Abstract: - Reversible logic has become one of the most promising research areas in the past few decades and has found its applications in several technologies; such as low power CMOS, nano-computing and optical computing. The problem of minimizing the number of garbage outputs is an important issue in reversible logic design. In this paper we propose a new 4×4 universal reversible logic gate. The proposed reversible gate can be used to synthesize any given Boolean functions. We also gain better improvements in terms of power and area when compared to conventional adders and multipliers. The implemented designs are simulated using NC launch and synthesized by RTL compiler. We also gain better improvements in terms of power and area when compared to conventional adders and multipliers. The implemented designs are simulated using NC launch and synthesized by RTL compiler. In this paper we have used Peres gate and the proposed Modified HNG (MHNG) gate to construct the reversible fault tolerant multiplier circuit

Keywords: Reversible logic, Garbage output, Garbage constant, Quantum Cost

1. INTRODUCTION

In modern VLSI systems power dissipation is very high due to rapid switching of internal signals. A part of this energy loss is due to switches and materials. The advancement in higher-level integration and fabrication process has emerged in better logic circuits and energy loss has also been dramatically reduced over the last decades. The combinational circuit dissipates KTlog2 [1] Joules of heat for every bit of information to be lasted, irrespective of the technology used. A gate is considered to be reversible only if for each and every input there is a unique output assignment. Hence there is a one to one mapping between the input and output vectors. Energy loss by Landauer limit is important because it is likely that the growth of heat generation due to information loss will be noticeable in future.

1.1 Garbage Outputs

The output of the Reversible gates which are not used further in the design, the efficient Reversible design must have less garbage bits.

1.2 Constant Inputs

The inputs of Reversible gates which are assigned to either logic „1" or logic „0",to obtained required Boolean expression. A good design should have minimal constant inputs.

1.3 Quantum Cost

Number of basic 2*2 Reversible gates used to implement required Reversible gates.

For Reversible gates 2*2 gates are the unit gates.
An efficient Reversible gate must have following features:
1. Total garbage outputs in the design as less as possible.
2. Design must be acyclic.
3. Minimization of the Reversible gates and constant inputs

On applying reversible computing we can move charges from one node to other with the help of oscillators and switches, hence saving both power and

time A gate is considered to be reversible only if for each and every input there is a unique output assignment. Hence there is a one to one mapping between the input and output vectors [2].

2. REVERSIBLE LOGIC:

A gate is considered to be reversible only if for each distinct input there is a distinct output assignment. Thus inputs to reversible gates can be uniquely determined from its outputs. Reversible logic is gaining importance in areas of CMOS design because of its low power dissipation. The traditional gates like AND, OR, XOR are all irreversible gates. Consider the case of traditional AND gate. It consists of two inputs and one output. As a result, one bit is lost each time a computation is carried out. According to the truth table there are three inputs (1, 0), (0, 1) and (0, 0) that corresponds to an output zero. A reversible logic gate must have the same number of inputs and outputs. In an n-output reversible gate the output vectors are permutation of the numbers 0 to 2n-1. Recovering the signal energy to the desired extent is possible using asymptotically[3],[4] adiabatic logic, where the energy is transferred inside the circuit avoiding any abrupt discharge of a high potential to ground.

It can realize non-balanced functions only with garbage outputs. Some of the major problems with reversible logic synthesis are fan outs cannot be used, and also feedback from gate outputs to inputs is not permitted [5]Features for any gate to become reversible gate as follows:

- Number of input and output lines must be the same.
- Feedback (loop) is not allowed in reversible logic.
- Fan-out is not allowed in reversible logic; Fan-out[6] is a term that defines the maximum number of digital inputs that the output of a single logic gate can feed.
- One of the major constraints in reversible logic is to minimize the number of reversible gates used.
- Minimizing the garbage outputs produced; Garbage output [7]refers to the output that is not used for further computations.

3. REVERSIBLE GATES

Several reversible gates have come out in the recent years. The most basic reversible gate is the Feynman gate and is shown in figure 1. It is the only 2x2 reversible gates available and is commonly used for fan out purposes. Consider the input B as constant. When B is zero, the gate acts as a copying gate or a buffer where both the output lines contain the input A. When B is one, the complement of A is obtained at the output Q. The 3x3 reversible gates [8] include Toffoli gate, Fredkin gate, new gate and Peres gate, all of which can be used to realize various Boolean functions. Fredkin gate is shown in figure 2.

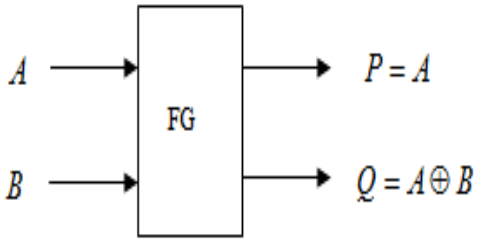

Figure 1: Feynman Gate

The Toffoli gate is a 3X3 gate has quantum cost of 5 and garbage outputs of 2. The Peres gate is also a 3X3 reversible gate whose quantum cost is 4 and garbage outputs are 2. Several 4x4 gates have been described in the literature targeting low cost and delay which may be implemented in a programmable manner to produce a high number of logical calculations. Minimizing the garbage outputs produced; Garbage output refers to the output that is not used for further computations. Garbage is the number of outputs added to make an n-input k output Boolean function ((n,k)function) reversible

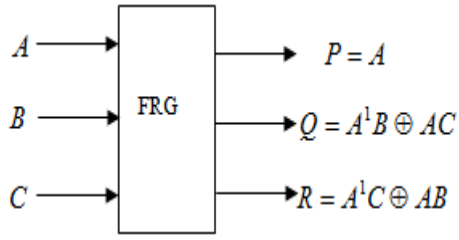

Figure 2: Fredkin Gate

Figure 3 shows the Peres gate. Some of the 3x3 gates are designed for implementing some important combinational functions in addition to the basic functions. Most of the above mentioned gates can be used in the design of reversible multiplier.

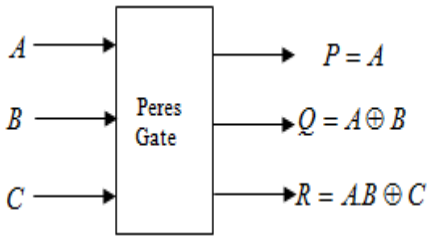

Figure 3: Peres Gate

The quantum cost and delay of the HNG is 6. When D = 0, the logical calculations produced on the R and S outputs are the required sum and carry-out operations for a full adder. The block diagram of the HNG is presented in Fig. 4.

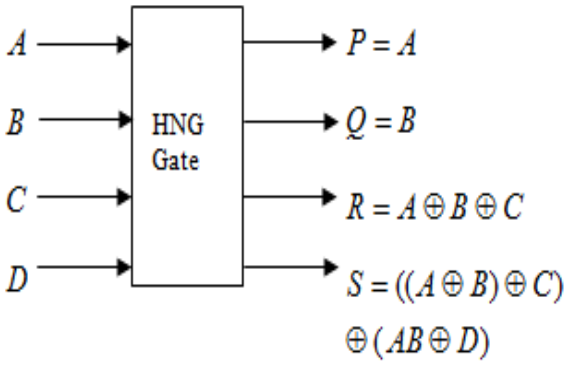

Figure 4: HNG Gate

4. REVERSIBLE MULTIPLIER

To compute product of two signed numbers we have used modified Baugh-Wooley approach [8]. Both logical and reversible multiplier design is divided into two parts: partial product generation circuit and then multi-operand addition circuit.

Design of Logical Multiplier:-

First to compute partial product, we used 17 AND 8 NAND employing the procedure given in figure 5. After generating partial products, next step is a multi-operand addition. We should add the bits of each column given in figure 5. To add these bits, we need FA and HA. We have to add these bits in the way that our circuit will give the best results. Figure 6 shows the way of adding these bits in our proposed circuit. The Wallace approach has been used to construct a circuit with less delay. To minimize delay in our proposed circuit, P9 is computed by inverting carry output from earlier FA (FA13).

The resulting circuit for multi-operand addition needs one 1-NOT gate, 4-HA and 16-FA. For the sake of simplicity, the proposed reversible multiplier is designed for 2- bit input operands. This can be extended to n*n bit multiplication. Using the reversible peres gate, 2*2 multiplier can be designed as shown in the figure below. This design requires six peres gates producing 11 garbage outputs. Consider A1, Ao be two bits of a number and B1,Bo be two bits of other number. Let Po, P1,P2,P3 be four output bits of multiplication.

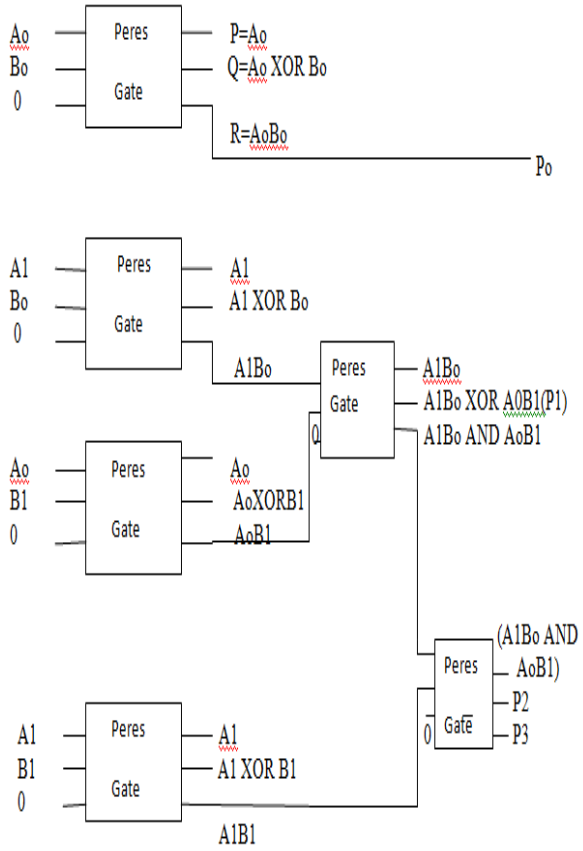

Figure 5: Proposed 2*2 reversible multiplier

Design of reversible multiplier:-

The operation of the 5x5 multiplier is depicted in figure 7. It consists of 25 partial product bits of the form. The reversible 5x5 multiplier circuit has two parts. First, the partial products are generated in parallel using Toffoli gate. We used 25 Toffoli gates to create 17 ANDs and 8 NANDs as shown in figure 6. The modified partial the

last low replace by Peres gate because Peres gate has quantum cost of 4 as shown if figure 6.

The reversible multiplier circuit design which has combined advantages of less power dissipation and timing delay can be used as the building block in the design of arithmetic logic units(ALU's) and other complex arithmetic[8] circuits. The number of garbage outputs, delay, power dissipation of reversible multiplier circuit can be reduced further by improvising the design. The proposed reversible multiplier placement and routing can be carried out by tool like cadence Encounter. Semicustom[15] design includes giving design specifications to schematic using Cadence's Virtuoso tool and verifying the functionality in SPECTRE. The obtained transient characteristics for the schematics and the circuit delays. The layouts for these circuits are designed using tool Assura and checked for DRC[14], ERC and LVS[9] match.

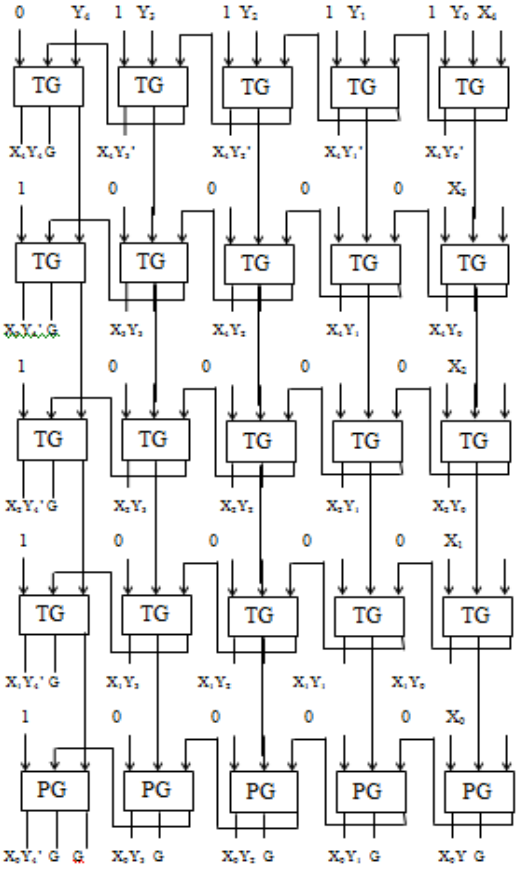

Figure 6: Modified Partial Product Generation by Toffoli Gates and Peres Gate

5. SIMULATION RESULT

The proposed reversible multiplier circuit is more efficient than the existing circuit presented by [10], [11], [12] and [13].. The proposed partial product is minimize 5 quantum cost in the design. Increase the number bit of the reversible multiplier circuit so reduced the quantum cost. Implementation of adder and multiplier in conventional and reversible logic stated, displayed the comparison among adder and multiplier both in area and power of them was determined by Table I and II .

Table I: Comparison of Power and Area between Reversible implementation and conventional design for CLA

Design	Area	Power(mw)
Conventional CLA	75	0.03
Reversible CLA	230	0.01

Table II: Comparison of Power and Area between Reversible implementation and conventional design for Array Multiplier

6. SCOPE FOR FUTURE WORK:

The Reversible adder circuits' design which has combined advantages of less chip area, improved power dissipation and timing delay can be used as the building blocks in the design of reversible multipliers, arithmetic logic unit (ALU), successive approximation registers etc... The number of garbage outputs, delay, and power dissipation of the reversible adder circuits can be reduced further by improvising the design.

7. CONCLUSION

In this paper we presented and successfully implemented Wallace reversible signed multiplier circuit. It is proved that not only the proposed

multiplier is better and optimized, compared to its existing counterparts with respect to the number of gates, garbage outputs, hardware complexity, and quantum cost. The simulated and synthesized results shows that reversible logic design is useful for low power digital circuits. We have been successful in verifying the advantages of reversible gates over basic gates circuits. This proposed multiplier consumes less power and has less worst case delay. A design of 2*2 reversible multiplier is successfully synthesized. The simulation of the design is done in cadence virtuoso 0.18um technology. The output waveform, power dissipation and worst case delay are shown. Multiplier circuit works with 1.8v supply. Simulation results are carried out by the NC launch and the power generation carried out by the RTL complier of CADENCE Tools.

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