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Design and implementation of Vedic Multiplier with adaptive hold logic

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Abstract: - In this paper we address the devise convention with the achievement of Vedic multiplier in spite of bypassing multiplier keeping in mind to improve the performance in terms of more speed and less power delay, with our existing design we have concentrated on completion of row and column by pass multiplier which consist of multi-level MUX's and also full adders for aging aware circuit. Since the additional usage of MUX results additional delay and power dissipation for existing design. The most significant aspect of the proposed method is that, the developed multiplier architecture is based on Vertical and Crosswise structure of Ancient Indian Vedic Mathematics. It generates all partial products and their sum in one step the proposed Vedic multiplier is coded in VHDL (Very High Speed Integrated Circuits Hardware Description Language), synthesized and simulated using HDL designer and precision synthesis tool.

Keywords: Ripple Carry (RC) Adder, Multiplication, Vedic Mathematics, Vedic Multiplier (VM), Urdhava Tiryakbhyam Sutra.

1. INTRODUCTION:

Digital multipliers are among the most critical arithmetic functional units in many applications, such as the Fourier transform, discrete cosine transforms, and digital filtering. The through put of these applications depends on multipliers, and if the multipliers are too slow, the performance of entire circuits will be reduced. In today's world low power issues have become a major significant factor in modern VLSI design. In fact, Low Power VLSI chips have emerged as highly in demand for designing any subsystem. Low power circuit is realized using both hardware and software approach.[12] The limited power capacity of the portable system has lead designers to more power aware designs. Energy efficient circuits are required because of the increasingly stringent demands for battery space and weight in portable multimedia devices, particularly in digital multipliers which are basic building blocks of digital signal processors. Besides adders, digital multipliers are the most critical arithmetic functional unit in many DSP applications such as in filters, Fourier transform and discrete cosine transform and in multiplier accumulate unit. Both array and parallel multipliers are in high demand because of their high execution speed and throughput. [5] The advantage of array multiplier is its regular structure; therefore layout becomes simple and it occupies less area since it has small size. In VLSI, the regular structures can be cemented one over another; this reduces the amount of mistakes and also reduces layout design. A basic multiplier can be divided into three parts partial product generation ,partial product addition and final addition .In this paper we present a low power ,low area design methodology for parallel array multiplier using carry save adder. Power dissipation is the most important parameter for portability & mobility and it is classified into dynamic and static power dissipation. Dynamic power dissipation arises when the circuit is overall consuming that means when it's operational, while static power dissipation arises when the circuit is inactive or is in a power down mode. There are three main components of power consumption in digital CMOS VLSI circuits [8].

1) Switching Power: arises because of the charging and discharging of the circuit capacitances during transistor switching. 2) Short Circuit Power: arises due to short circuit current flowing from power supply to ground during transistor switching.

3) Static Power: arises when the circuit is in stable state due to static and leakage currents flowing. The first two are referred to as dynamic power as the power is consumed dynamically while the circuit is changing states.[8] In designing a low power CMOS 1 bit full adder, the emphasis will on the following areas [10].

Keywords-- Vedic multiplier, multi level MUX's, aging aware circuit, arrays based adder's.

[1] To reduce the total number of transistor count in the design and to reduce the load capacitance also to reduce

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the total number of parasitic capacitances in internal nodes
[2] To save the dynamic power consumption by lowering the switching activity
[3] To remove some direct paths from the power supply to ground to save the short circuit power dissipation.
[4] To reduce the appearance of glitches which leads to unnecessary power dissipation also leads to fault circuit operation due to spurious transitions especially in low voltage operation system.
[5] In order to build a low power full adder, all the internal nodes in the circuit must possess full voltage swing at the output nodes.
[6] To build the low voltage full adder design because the power supply voltage is the crucial factor in reducing power dissipation [8].
In order to reduce the power consumption of the adders any one of the above factors of the circuit need to be reduced. In nanometer scale leakage power dominates the dynamic power and static power due to hot electrons. So the concentration is on trade off power in array multipliers.

II. CONVENTIONAL MULTIPLIERS

A) Column-Bypassing Multiplier
A column-bypassing multiplier is an improvement on the normal array multiplier (AM). The AM is a fast parallel AM and is shown in Fig. 1. The multiplier array consists of (n−1) rows of carry save adder (CSA), in which each row contains (n −1) full adder (FA) cells. Each FA in the CSA array has two outputs: 1) the sum bit goes down and 2) the carry bit goes to the lower left FA. The last row is a ripple adder for carry propagation.

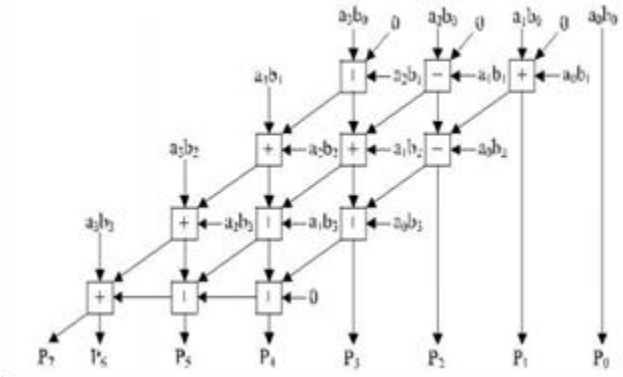

Fig.1. 4 × 4 normal AM

The FAs in the AM are always active regardless of input states. In, a low-power column-bypassing multiplier design is proposed in which the FA operations are disabled if the corresponding bit in the multiplicand is 0. Fig. 2 shows a 4×4 column-bypassing multiplier. Supposing the inputs are 10102 * 11112, it can be seen that for the FAs in the first and third diagonals, two of the three input bits are 0: the carry bit from its upper right FA and the partial product aibi. Therefore, the output of the adders in both diagonals is 0, and the output sum bit is simply equal to the third bit, which is the sum output of its upper FA.
Hence, the FA is modified to add two tristate gates and one multiplexer. The multiplicand bit ai can be used as the selector of the multiplexer to decide the output of the FA, and ai can also be used as the selector of the tristate gate to turn off the input path of the FA. If ai is 0, the inputs of FA are disabled, and the sum bit of the current FA is equal to the sum bit from its upper FA, thus reducing the power consumption of the multiplier. If ai is 1, the normal sum result is selected.

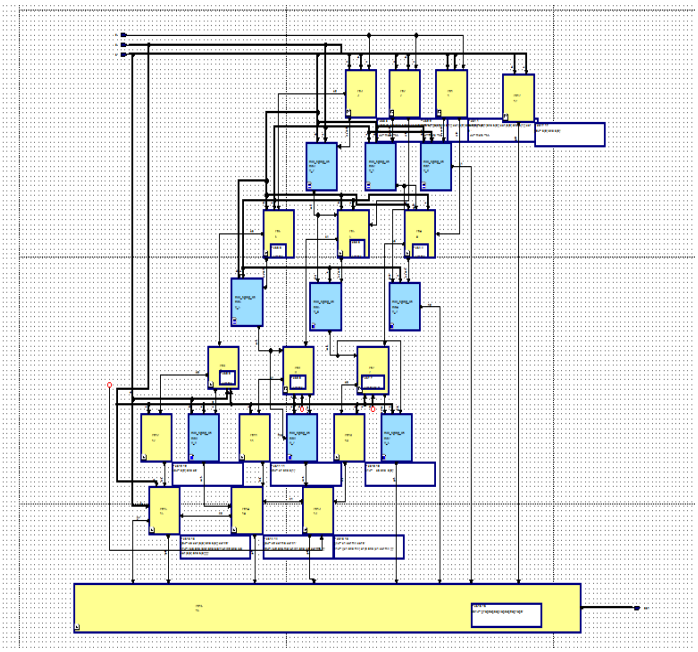

Fig.2. 4 × 4 column-bypassing multiplier.

B) Row-Bypassing Multiplier
A low-power row-bypassing multiplier is also proposed to reduce the activity power of the AM. The operation of the low-power row-bypassing multiplier is similar to that of the low-power column-bypassing multiplier, but the selector of the multiplexers and the tristate gates use the multiplicator. Fig. 3 is a 4 × 4 row-bypassing multiplier. Each input is connected to an FA through a tristate gate. When the inputs are 11112 * 10012, the two inputs in the first and second rows are 0 for FAs. Because b1 is 0, the multiplexers in the first row select aib0 as the sum bit and select 0 as the carry bit. The inputs are bypassed to FAs in the second rows, and the tristate gates turn off the input paths to the FAs. Therefore, no switching activities occur in the first-row FAs; in return, power con-

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sumption is reduced. Similarly, because b2 is 0, no switching activities will occur in the second-row FAs. However, the FAs must be active in the third row because the b3 is not zero.

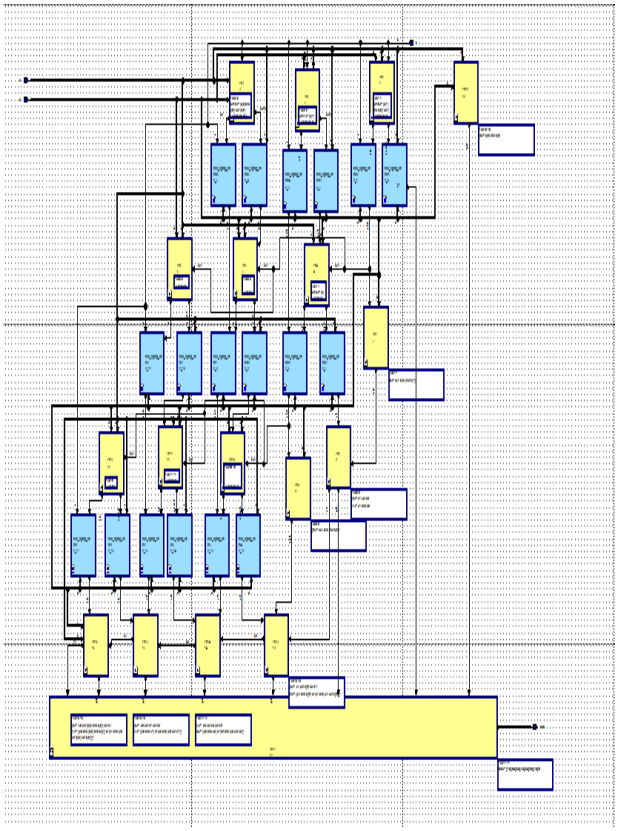

Fig.3. 4 x 4 row bypassing multiplier

Fig.3. 4 x 4 row bypassing multiplier the proposed aging-aware reliable multiplier design. It introduces the overall architecture and the functions of each component and also describes how to design AHL that adjusts the circuit when significant aging occurs.

A) Array Multiplier

Proposed Array Multiplier In the proposed array multiplier the full adder cells is implemented using 10T full adder cell as shown in Fig4. The 10T full adder circuit is designed using inverted based 4T XOR gates in the designed full adder cell and shows remarkable improvements in power and delay. [3]This 1 bit full adder cell has less power consumption as it has no direct path to ground .The elimination of a path to the ground reduces power consumption .It is observed that the newly designed 10-T adder has no direct path to the ground. The charge stored at the load capacitance is reapplied to the control gates. The circuit produces full-swing at the output nodes. The circuit even fails to provide so for the internal nodes. The combination of not having a direct path to ground and the re-application of the load charge to the control gate makes the energy-recovering full adder an energy efficient design. Due to multiple threshold problems it cannot be cascaded at low power supply. Also the circuit becomes slower as the power consumption by the circuit reduces. Thus implementing the array multiplier using 10T full adder cell shows to be more power and area efficient when compared with the 16T full adder cell

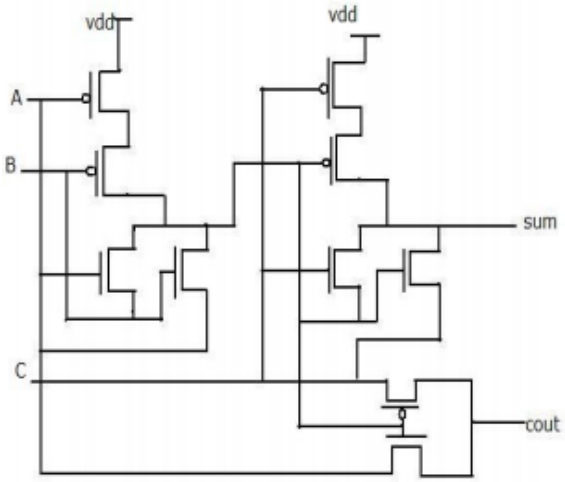

Fig4.10t Full Adder Cell

III. PROPOSED VEDIC MULTIPLIER WITH AHL URDHVA TIRYAGBHYAM

A. Vedic Mathematics

The proposed Vedic multiplier is mainly depending on the Vedic multiplications formula (sutras). Vedic multiplier canbe deals with more basic operations as well as not simple mathematical operations. In this Vedic multiplier the basic arithmetic operation are done in a simple and powerful manner. It is unique method of calculation and done by simple principles and rules. Vedic mathematics is mainly depends on 16 sutras. These sutras have been conventionally used for the multiplications of two numbers in decimal number system and it deals with several applications in mathematics like arithmetic, trigonometry, algebra etc.

B. UrdhvaTiryakbhyam

In this paper, UrdhvaTiryakbhyam sutras are used in the Vedic multiplier. Urdhva means updown or vertically and Tiryakbhyam means crosswise. In this sutras, the biased products and their summation occur in the multiplication are determined parallel shown in the Fig.1. Then the multiplier is not dependent on the frequency of clock occur in the processor. Normally, the microprocessor operations are operating at increase in high clock frequency and it leads to increasing the processing pow-

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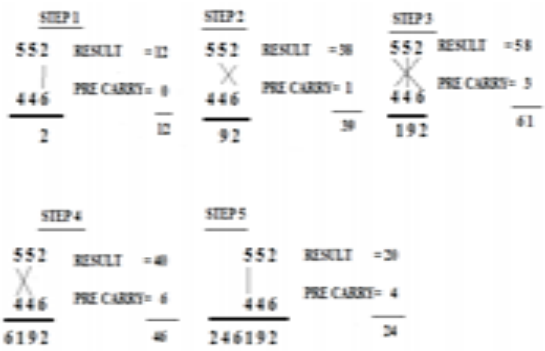
er. But in the Vedic multiplier, the microprocessor designer can be easily detecting these problems to avoid the failure of device ref [11]-[12].



Multiplications of Two Decimal Numbers

IV. PROPOSED ARCHITECTURE

In this section describes the details of proposed Vedic multiplier using AHL. It has the total architecture and describes the operations of each block. The proposed architecture is shown in the Fig.2, which includes 4x4Vedic multiplier, razor flip-flop and an AHL circuit.

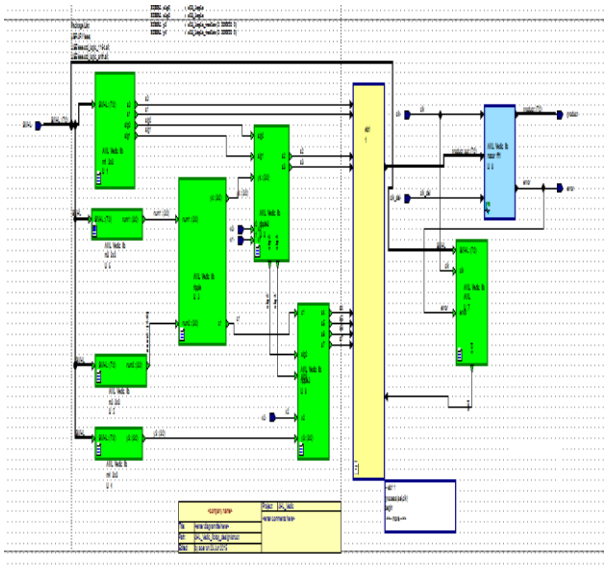


Fig 5 proposed Vedic multiplier with adaptive hold logic

A. Razor Flip-flop

Razor flip-flop consists of a main flip-flop, shadow latch, xor and multiplexer ref [13]. When D flip-flop seize the execution of regular clock signal and the shadow latch seizes the execution of delayed clock signal. The normal clock signal is faster than delayed clocked signal.

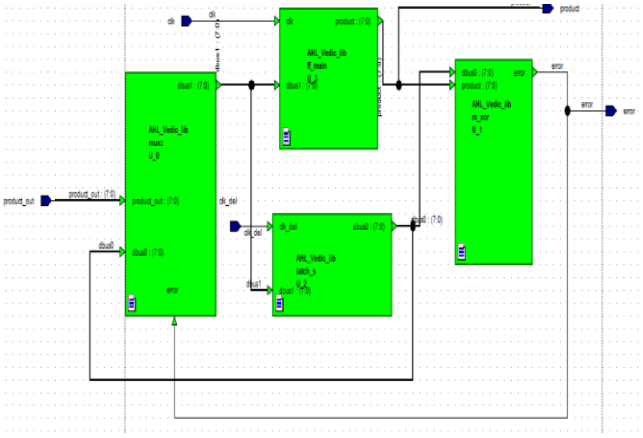


Fig.6. Razor Flip-flop

The path delay of the present operation beyond the cycle period and the main flip-flop hold the incorrect result. Razor flip-flop notify the AHL whether the error is occurring in the circuit or not. If error occurs, it gives signal 1 to make known the system to reexecute the operation. It denotes the operations that are taken to be two cycle pattern. So, the razor flip-flop is used to detect the error occur in the circuit.

B. Adaptive Hold Logic

Adaptive hold logic consists of indicator, multiplexer, 2 judging block and D flip-flop. When the cycle period is very short, then the Vedic multiplier can't be able to finish these operations. So, it causes timing violations. It caught by razor flip-flop and it generate error signal.

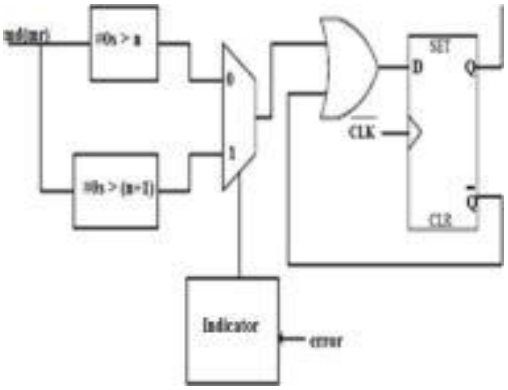


Fig.7. Adaptive Hold Logic

Judging block first have output is 1, if multiplicand (multiplicator) have number of zeros is larger than n. Similarly, judging block second have output is 1, if multiplicand (multiplicator) have number of zeros is larger than n+1. These both block are decide whether input pattern require one or two clock cycles. But at a time, one judging block will be chosen. When the model re-

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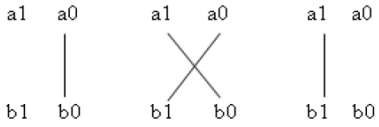
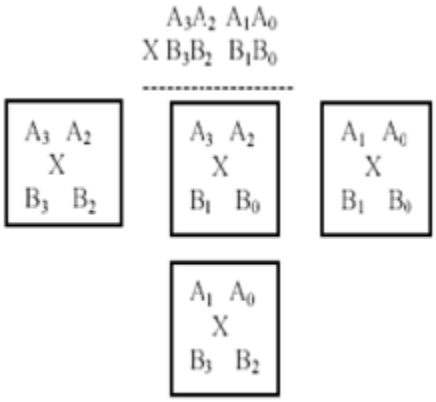
quires single cycle, the multiplexer output is 1 and then signal of gating also become 1. Then, the D flip-flop latches the new data in the next cycle. Similarly, the multiplexer output have 0 then the signal of gating becomes 0 and to unfit the clock signal of the input flip-flop in the next cycle.

C. Operation of Vedic Multiplier using AHL

When input pattern arrives, the Vedic multiplier and AHL perform their operation at a same time. The multiplicand (multiplicator) have number of zeros, the adaptive hold logic circuit decide it takes 1 or 2 cycles. After finishing the operation of Vedic multiplier and it goes to razor flip-flop. The razor flip-flop checks whether there have any path delay timing violation. So, if any timing violation occurs it executes the operation by using two cycle's pattern and it indicate to the AHL. Finally our architecture minimizes the timing violation of the circuit.



Logic for 2X2 Multiplication:



Logic for 4x4 Design Units for Vedic Multipliers:

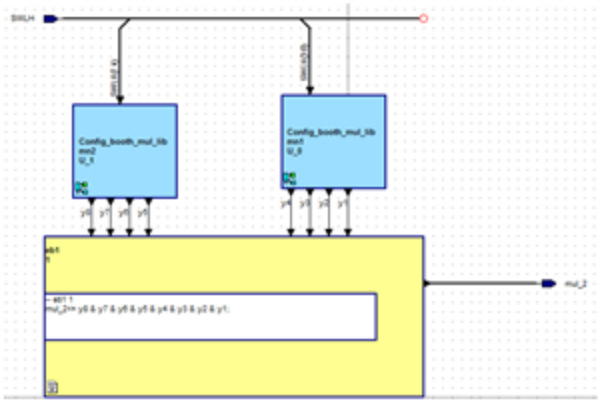


Fig 7: Representing the Vedic multiplier for 2x2 algorithm

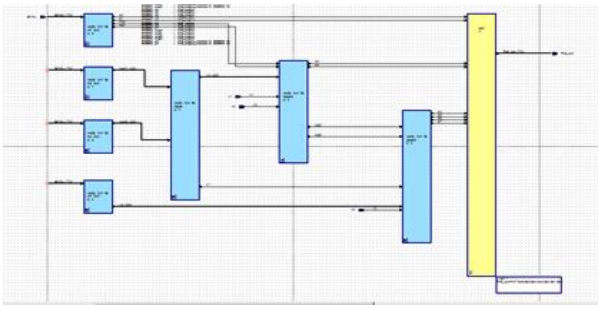


Fig 8: Representing the Vedic multiplier for 4X4 algorithm

V.RESULT AND DISCUSSION

For the overall analyses of the Vedic multiplier using adaptive hold logic. We get the following reduction in area using HDL Designer EDA tool. We analyze the Vedic multiplier using AHL as compared the conventional array multipliers. By using AHL, the circuit minimizes the timing waste in the multiplier. So, it reduces the area and delay in the circuit. The above tabulation depicts that the area and delay analyses for 4x4vedic multiplier by simulation. The comparison proves that by the use of 4x4 Vedic multiplier with AHL area got reduced.

Area report of aging aware reliable multiplier with adaptive hold logic

```
*************************************************************
Device Utilization for 4VLX25SF363
*************************************************************
Resource                    Used    Avail   Utilization
-------------------------------------------------------------
IOS                         19      240     7.92%
Global Buffers              2       32      6.25%
LUTs                        118     21504   0.55%
CLB Slices                  59      10752   0.55%
Dffs or Latches             49      21504   0.23%
Block RAMs                  0       72      0.00%
DSP48s                      0       48      0.00%
-------------------------------------------------------------
```

Area report of Vedic multiplier with adaptive hold logic

```
**********************************************************
Device Utilization for 3S250ETQ144
**********************************************************
Resource                    Used    Avail   Utilization
----------------------------------------------------------
IOs                         22      108     20.37%
Global Buffers              2       24       8.33%
LUTs                        53      4896     1.08%
CLB Slices                  27      2448     1.10%
Dffs or Latches             24      5112     0.47%
Block RAMs                  0       12       0.00%
Block Multipliers           0       12       0.00%
----------------------------------------------------------
```

Comparison Table 1.

	Aging aware reliable multiplier	Vedic multiplier
Io's	19	22
Global buffers	2	2
LUT'S	118	63
CLB slices	59	32
Dff's or latches	49	24
Total	247	143

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