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Area Efficient and High Speed Vedic Multiplier Using Different Compressors

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Abstract: - The performance of trending technology in VLSI field supports ongoing expectation for high speed Processing and lower area consumption. It is also a well known fact that the multiplier unit forms an integral part of processor design. Due to this regard, high speed multiplier architectures become the need of the day. The proposed design has reduced area, LUT tables and increase the speeds compared with the regular compressor based multiplier. The multiplication sutra between these 16 sutras is the Urdhva Tiryakbhayam sutra which means vertical and crosswise. In this paper it is used for designing a high speed, low power 4*4 multiplier. The proposed system is design using VHDL and it is implemented through Xilinx ISE 14.2. The design and experiments were carried out on a Xilinx Spartan 3e series of FPGA and the timing and area of the design, on the same have been calculated.

Keywords – Ripple Carry Adder, half adder, full adder, Compressors, high speed multiplier, Urdhwa Tiryakbhyam Sutra, Vedic Mathematics.

1. INTRODUCTION

The speed of a processor greatly depends on its multiplier's performance. This in turn increases the demand for high speed multipliers, at the same time keeping in mind low area and moderate power consumption [1]. Over the past few decades, several new architectures of multipliers have been designed and explored. The development in processor is based on the function of the multipliers. The multiplier that is being designed should meet with various criteria like low power consumption and lesser area occupation. For several years, new modified architectures of multipliers are being introduced and implemented successfully.The circuit has an uncontrolled multiplication and division factor range and short lock time. A short power method has been incorporated to ensure that the overall power consumption of the circuit is low. The circuit has been premeditated in TSMC 65nm CMOS process for an input allusion time of 0.01ns and has been tested with indiscriminate multiplication factor values, we present a novel architecture to perform high speed multiplication using ancient Vedic math's techniques. A new high speed approach utilizing 4:2 compressors and novel 7:2 compressors for addition has also been incorporated in the same and has been discovered. Upon evaluation, the compressor based multiplier introduced in this paper, is nearly two times faster than the popular methods of multiplication [2].

The feature of Vedic mathematics is that every sub products needed for multiplication are obtained even before the real operations even begin [3]. The results of such preproduction are then added to get the final result [3]. This is a major criterion that results in a really high speed multiplication [5]. The new approach discuss a novel method to additionally improve the speed of the Vedic mathematics multiplication by means of substituting the already existing full adders and half adders of the Vedic mathematics supported multipliers with compressors . These compressors are nothing but, logical circuits that could add more than 3 bits at a time in contrast with a full adder, additionally

this could also do the same with a much more reduced number of gate counts and greater speed similar to a basic full adder circuit [4].

The Vedic methods multipliers have been altered and advanced for better are direct, and truly amazing in their efficiency [6]. The increased complexity of various simplicity. Research is being carried out in many parts, functions, demands not only faster multiplier chips but also including the effects on children who learn Vedic math's and the smarter and efficient multiplying algorithms that can be development of new, powerful but easy applications executed in the chips. It is up to the necessity of the hour and Vedic sutras in geometry, calculus, computing etc. But the real the application on to which the multiplier is implemented and beauty and efficiency of Vedic mathematics cannot be fully what tradeoffs need to be reflected. Generally, the efficiency valued without actually practicing the system. The speed of a processor highly depends on its multiplier's performance.

2. URDHAVA TIRYAKBHYAM METHOD

Vedic Mathematics can be divided into 16 different sutras to perform mathematical calculations. Among these the Urdhwa Tiryakbhyam preferred algorithms for performing multiplication. The words"Urdhwa Tiryakbhyam originated from Sanskrit words Urdhwa and Tiryakbhyam which mean vertically and crosswise respectively [6]. The main advantage of utilizing this algorithm in comparison with the existing multiplication techniques, is the fact that it utilizes only logical AND operations, half adders and full adders to complete the multiplication operation. Also, the partial products required for multiplication are generated in parallel and prior to the actual addition thus saving a lot of processing time.

Let us consider two 8 bit numbers A7-A0 and B7-B0, where 0 to 7 represent bits from the Least Significant Bit (LSB) to the Most Significant Bit (MSB). P0 to P15 represent each bit of the final computed product. It can be seen from equation (1) to (15), that P0 to P15 are calculated by adding partial products, which are calculated previously using the logical AND operation. The individual bits obtained from equations (1) to (15), in turn when concatenated produce the final product of multiplication which is depicted in (16).The carry bits generated during the calculation of the individual bits of the final product are represented from C1 to C30. The carry bits generated in (14) and (15) are ignored since they are superfluous.

$$P0 = A0 * B0 \quad (1)$$

$$C1P1 = (A1 * B0) + (A0 * B1) \quad (2)$$

$$C3C2P2 = (A2 * B0) + (A0 * B2) + (A1 * B1) + C1 \quad (3)$$

$$C5C4P3 = (A3 * B0) + (A2 * B1) + (A1 * B2) + (A0 * B3) + C2 \quad (4)$$

$$C7C6P4 = (A4 * B0) + (A3 * B1) + (A2 * B2) + (A1 * B3) + (A0 * B4) + C3 + C4 \quad (5)$$

$$C10C9C8P5 = (A5 * B0) + (A4 * B1) + (A3 * B2) + (A2 * B3) + (A1 * B4) + (A0 * B5) + C5 + C6 \quad (6)$$

$$C13C12C11P6 = (A6 * B0) + (A5 * B1) + (A4 * B2) + (A3 * B3) + (A2 * B4) + (A1 * B5) + (A0 * B6) + C7 + C8 \quad (7)$$

$$C16C15C14P7 = (A7 * B0) + (A6 * B1) + (A5 * B2) + (A4 * B3) + (A2 * B5) + (A1 * B6) + (A0 * B7) + C9 + C11 \quad (8)$$

$$C19C18C17P8 = (A7 * B1) + (A6 * B2) + (A5 * B3) + (A4 * B4) + (A3 * B5) + (A2 * B6) + (A1 * B7) + C10 + C12 + C14 \quad (9)$$

$$C22C21C20P9 = (A7 * B2) + (A6 * B3) + (A5 * B4) + (A4 * B5) + (A3 * B6) + (A2 * B7) + C13 + C15 + C17 \quad (10)$$

$$C25C24C23P10 = (A7 * B3) + (A6 * B4) + (A5 * B5) + (A4 * B6) + (A3 * B7) + C16 + C18 + C20 \quad (11)$$

$$C27C26P11 = (A7 * B4) + (A6 * B5) + (A5 * B6) + (A4 * B7) + C19 + C21 + C23 \quad (12)$$

$$C29C28P12 = (A7 * B5) + (A5 * B6) + (A5 * B7) + C22 + C24 + C26 \quad (13)$$

$$C30P13 = (A7 * B6) + (A6 * B7) + C25 + C27 + C28 \quad (14)$$

$$P14 = (A7 * B7) + C29 + C30 \quad (15)$$

$$P15 = (A7 * B7) \quad (16)$$

The black circles indicate the bits of the multiplier and multiplicand, and the two-way arrows indicate the bits to be multiplied in order to arrive at the individual bits of the final product. As mentioned earlier, the partial products obtained are added with the help of full

adders and half adders. It can be seen, from equation (1) to (16) that in few equations there is a necessity of adding more than 3 bits at a time.

This leads to additional hardware and additional stages, since the full adder is capable of adding only 3 bits at a time. In the next section two different types of compressor architectures are explored which assist in adding more than 3 bits at a time, with reduced architecture and increased efficiency[7] in terms of speed.

3. COMPRESSOR BASED ADDERS

Several 4-2 and 5-2 compressor architectures have been reported so far [8], [9]. The main drawback associated with these conventional compressors is that the result generated is not in proper binary form and one more half adder/ full adder is required to get the final results, thereby increasing the area and power dissipation. Moreover, due to uneven delay profiles of the outputs arriving from different input paths, a lot of glitches are generated. Since here a number of adders are used, compressor adders used which replaces the half adders and full adders and thus increase the efficiency of the computational speed of adding 4 bits at a time or more than that. There are a lot of compressor based adders used but here 4:2 compressor adders are used [10].

A compressor adder is a logical circuit which is used to improve the computational speed of the addition of 4 or more bits at a time. Compressors can efficiently replace the combination of several half adders and full adders, thereby enabling high speed performance of the processor which incorporates the same. The compressor adder used in this paper is a 4:2 compressor adder. A lot of research in the past has been carried out on the same.

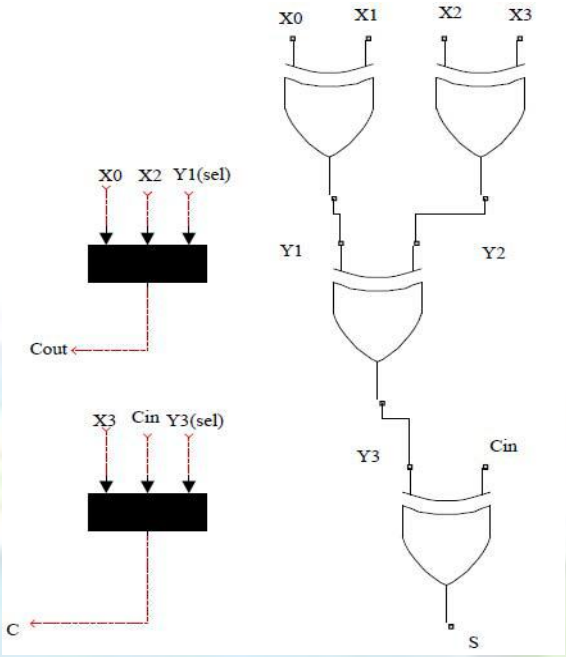


Fig. 1:Gate level diagram of 4:2 Compressor

Moreover, due to uneven delay profiles of the outputs arriving from different input paths, a lot of glitches are generated. To overcome these problems associated with the conventional compressors, higher order compressors proposed have been used in the design. These compressors have been designed as counter of „1" s at the input bits. The compressor called 4:2compressor is used for adding 4 bits along with one carry which results in producing a 3 bit number. Comparing this compressor with conventional full adders and half adders which is used for adding 5 bits, the critical path of compressor is smaller in size than used in conventional adders[6]. The internal gate level diagram of a 4:2 compressor is shown in fig 1. As it can be observed that the propagation delay of a full adder is 2tp and half adder has a propagation delay of tp while the propagation delay of 4:2 compressor is 3tp. It is seen that speed also increases by a 66.6% while comparing this with the conventional half and full adder circuits.The efficiency attained by this compressor is much more increased than the conventional method of adding nine bits at an instance using full and half adders and is 1.05 times speeder than existing method.

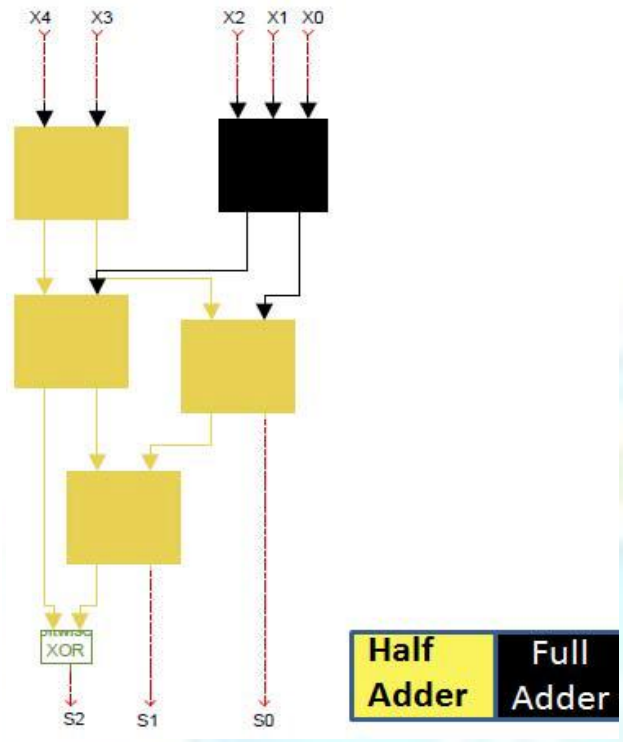


Fig. 2:. 4:2 Compressor using full adders and half adders

4. URDHWATIRYAKBHYAM MULTIPLIER USING COMPRESSOR:

Usually urdhwa approach of multiplication uses several number of half adders and full adders which adds the intermediately occurring partial products which results in increase in propagation delay. And hence here the new approach is to combine this compressor with the Urdhwa multiplication resulting in a compr iryakbhyam multiplier. The hardware architecture of the proposed multiplier requires only twelve parallel stages when comparison with conventional method which uses fifteen stages. So this proves to be a major enhancement in high speed multiplier design. Analysis of this approach proves that this uses only logical XOR operation resulting in reduced area.

The block diagrams of 4-3, 5-3 and 6-3 compressor contains three sub-units: two adder units and a Carry Look Ahead adder (CLA)[11] unit for parallel addition of the outputs of the adder units. The 7-3 compressor is implemented using 4-3 compressor, a full adder and a CLA unit.

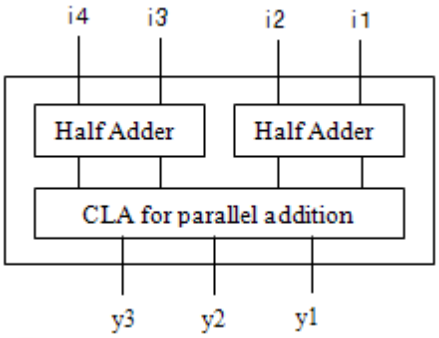


Fig.3. Block diagram of a 4-3 Compressor

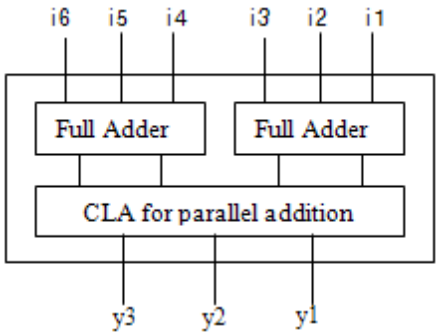


Fig.4. Block diagram of a 5-3 Compressor

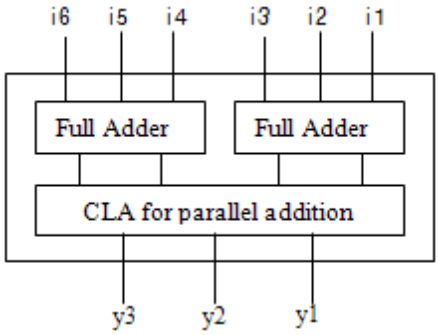


Fig.5. Block diagram of a 6-3 Compressor

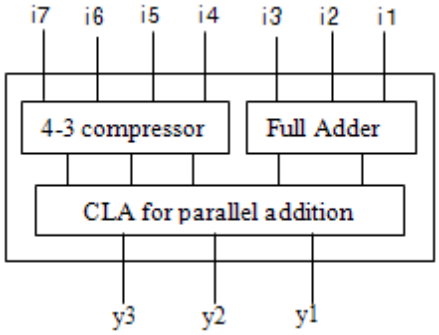


Fig.6. Block diagram of a 7-3 Compressor

In the earlier compressor based Vedic Multiplier [4], a large number of stages are required to add the partial products to obtain the final results. The 4-2 and 7-2

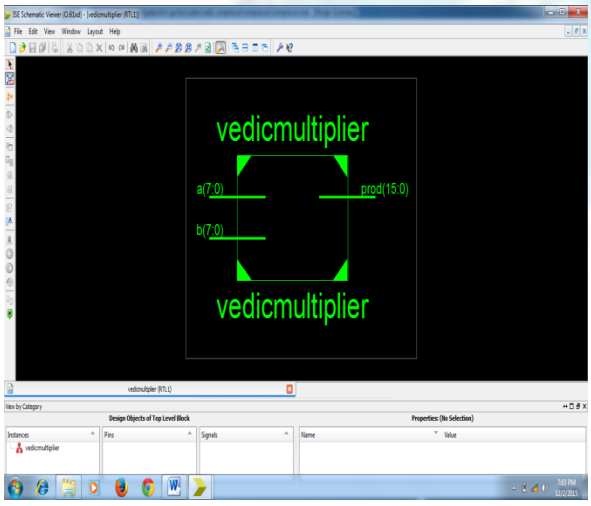
compressors are utilized only in the first two stages of the multiplier while the following eleven stages employ only full adder and half adder thereby increasing the reduction stages to thirteen .This leads to increased area and power consumption.In the proposed multiplier architecture, the higher order compressors have been used intelligently so that the partial products are added in only two stages to obtain the final result and hence giving an area efficient and low power consuming design. Also, compressors and adders are employed such that minimum number of outputs is generated. For example in column 5, there are 7 partial products to be added. These could be added using a 4-3 compressor and a full adder thereby generating five output bits. But instead of this a 7-3 compressor has been used which will generate only 3 output bits.

5. RESULTS

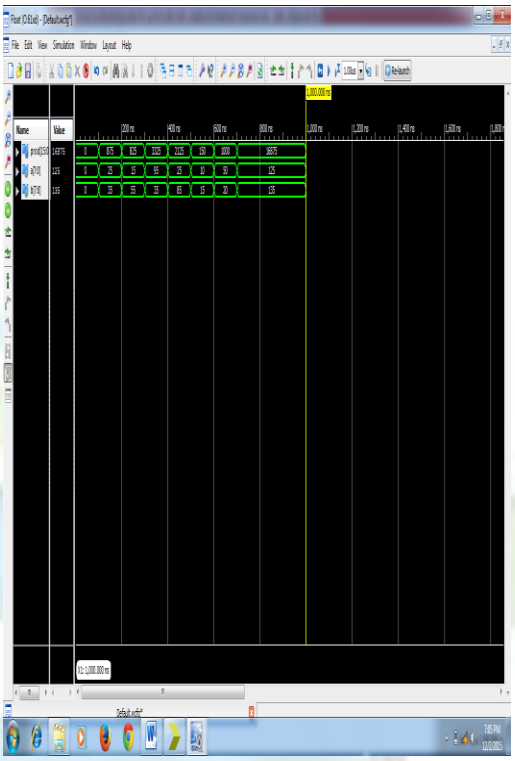
In order to perform a comparison, various popular multipliers Urdhwa multiplier and also the compressor based Urdhwa multiplier were implemented on a Xilinx Spartan 3e – XC3S500E FPGA using VHDL as the RTL language with the help of Xilinx Project Navigator 14.2.

The codes were synthesized. Unoptimized speed and area parameters were compared. The Spartan 3e FPGA used for the experiments has a speed grade of -5 and package CP132.

RTL SCHEMATICS



OUTPUT



6. CONCLUSION

The proposed compressor adder results in improvement in all three factors: speed, delay and power. The delay and power are reduced by a factor of 0.2 and 0.4 respectively while the speed is improved by a factor of 2 in 16 bit case. Vedic multiplier has the greatest advantage as compared to other multipliers over gate delays and regularity of structures. Speed in Vedic multiplier for 16 x 16 bit number is 155.96MHz while the speed in regular multiplier is 138.20MHz respectively. Instead of using full adder and half adder compressor adder is efficient. Thus this multiplier shows the highest speed among conventional multipliers. It has these advantages to prefer a best multiplier. As a future work compressor based Urdhwa multiplier was successfully designed with minimum area, power and high speed. Then the focus is to test a designed Vedic multiplier circuit using logic BIST. To reduce the overall power dissipation by using low transition LFSR for high speed CUT.

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