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Design and Implementation of LUT Optimization Using APC-OMS System

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Abstract: The multiplication is major arithmetic operation in signal processing and in ALU's .The multiplier uses look-up-table (LUT) as memory for their computations. However, we do not find any significant work on LUT optimization for memory-based multiplication. A new approach to LUT design was presented, where only the odd multiple storage (OMS) scheme. In addition to that the antisymmetric product coding (APC) approach, the LUT size is reduced to half and provides a reduction. When APC approach is combined with the OMS technique, the two's complement operations could be simplified since the input address and LUT output could always be transformed into odd integers, and thus reduces the LUT size to one fourth of the conventional LUT. The proposed LUT multipliers for word size L=W=5 bits are coded in VHDL and synthesized in Xilinx 14.2. It is found that the proposed LUT-based multiplier involves comparable area and time complexity for a word size of 5-bits.

Index Terms: Digital signal processing (DSP) chip, lookup table (LUT)-based computing, memory-based computing.

1. INTRODUCTION

Digital signal processing algorithms typically require a large number of mathematical operations to be performed quickly and repetitively on a set of data. Signals are constantly converted from analog to digital, manipulated digitally, and then converted again to analog form, as diagrammed below. Many DSP applications have constraints on latency; that is, for the system to work, the DSP operation must be completed within some fixed time, and deferred processing is not viable. Digital signal processing:

In-order to reach a certain criteria memory based computation plays a vital role in DSP (digital signal processing) application.

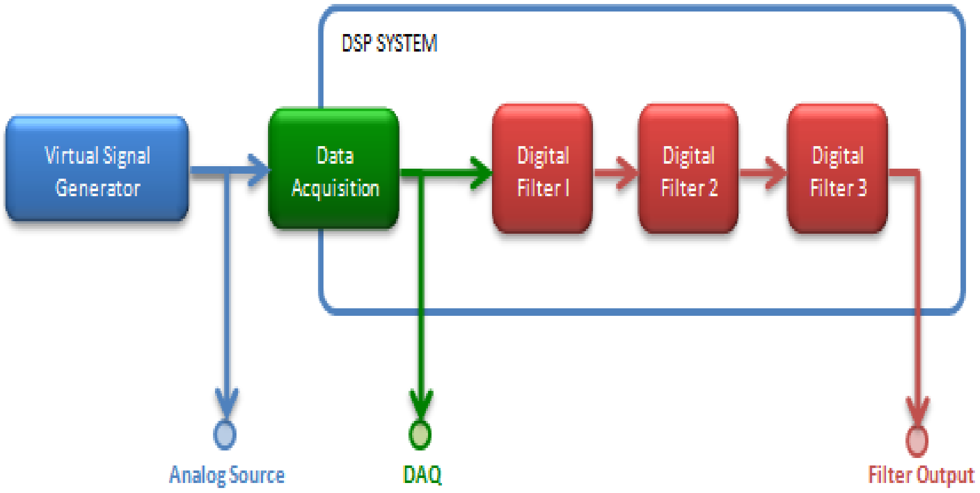


Fig 1. DSP System Framework

FILTER DESIGNING:

Finite impulse response (FIR) digital filter is widely used as a basic tool in various signal processing and image processing applications. The order of an FIR filter primarily determines the width of the transition-band, such that the higher the filter order, the sharper is the transition between a pass-band and adjacent stop-band. Many applications in digital Communication (channel equalization, frequency channelization), speech processing (adaptive noise cancelation), seismic signal processing (noise elimination), and several other areas of signal processing require large order FIR filters. Since the number of multiply-accumulate. (MAC) operations required per filter output increases linearly with the filter order, real-time implementation of these filters of large orders is a challenging task. Several attempts have, therefore, been made and continued to develop low- complexity dedicated VLSI systems for these filters.As the scaling in silicon devices has progressed over the last four decades, semiconductor memory has become cheaper, faster and more power-efficient. According to the projections of the international technology roadmap for semiconductors (ITRS), embedded memories will continue to have dominating presence in the system-on-chip (SoC), which may exceed 90%, of total SoC content. It has also been found that the transistor packing density of SRAM is not only high, but also increasing much faster than the transistor density of logic devices.

1.1 BINARY MULTIPLICATION:

Multiplication in binary is similar to its decimal counterpart. Two numbers A and B can be multiplied by partial products: for each digit in B, the product of that digit in A is calculated and written on a new line, shifted leftward so that its rightmost digit lines up with the digit in B that was used. The sum of all these partial products gives the final result.

1.2 FIR filter architecture:

The objectives of this work are:

•Multiplying two binary numbers one number is fixed X[4:0] and another variable 'A'

•Using APC-OMS combined LUT design for themultiplication of W-bit fixed coefficient A with 5-bit input X.

•Number of calculations reduced and memory required is less to perform multiplication. For 16- and 32-bit word sizes, respectively, it offers more than 30%

and 50% of saving in area-delay product over the corresponding CSD multipliers.

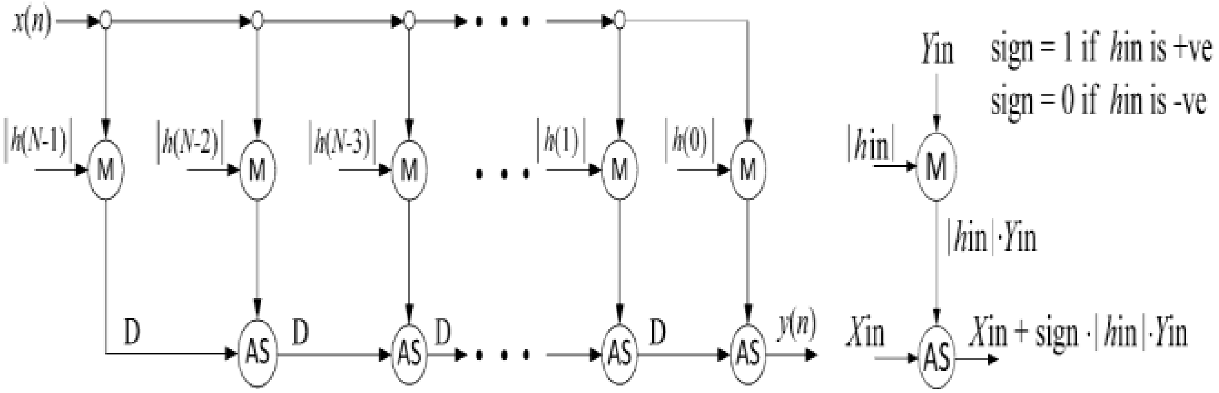


Fig 2.FIR filter architecture

1.3 ANTI -SYMMETRIC PRODUCT CODING:

Anti symmetric product coding is the technique used to process the multiplication based on LUT multiplication which reduces the size of conventional lut by 50 % .The anti symmetric product coding is based on the antisymmetric coding i.e the 2's complement phenomenon which is used to reduce the LUT size by half.For simplicity of presentation, we assume both X and A to be positive integers.2 The product words for different values of X for L = 5 are shown in Table I. It may be observed in this table that the input word X on the first column of each row is the two's complement of that on the third column of the same row. In addition, the sum of product values corresponding to these two input values on the same row is 32A. Let the product values on the second and fourth columns of a row be u and v, respectively. Since one can write u = [(u + v)/2 - (v - u)/2] and v = [(u + v)/2 + (v - u)/2], for (u + v) = 3 2 A, The APC approach, although providing a reduction in LUT size by a factor of two, incorporates substantial overhead of area and time to perform the two’s complement operation of LUT output for sign modification and that of the input operand for input mapping. However, we find that when the APC approach is combined with the OMS technique, the two’s complement operations could be very much simplified since the input address and LUT output could always be transformed into odd integers. However, the OMS technique in [9] cannot be combined with the APC scheme in [10], since the APC words generated according to [10] are odd numbers. Moreover, the OMS scheme in [9] does not provide an efficient implementation when combined with the APC technique. In this brief, we therefore present a different form of APC and combined that with a modified form of the OMS scheme for efficient memory- based multiplication.

The product values on the second and fourth columns of Table I therefore have a negative mirror symmetry. This behavior of the product words can be used to reduce the LUT size, where, instead of storing u and v, only [(v - u)/2] is stored for a pair of input on a given row. The 4-bit LUT addresses and corresponding coded words are listed on the fifth and sixth columns of the table, respectively. Since the representation of the product is derived from the anti-symmetric behavior of the products, we can name it as anti-symmetric product code.

The 4-bit address X'= x3'x2'x1'x0' of the APC word is given by X' = XL, if x4 = 1=X'L , if x4 = 0 where XL = (x3x2x1x0) is the four less significant bits of X, and XL' is the two's complement of XL.

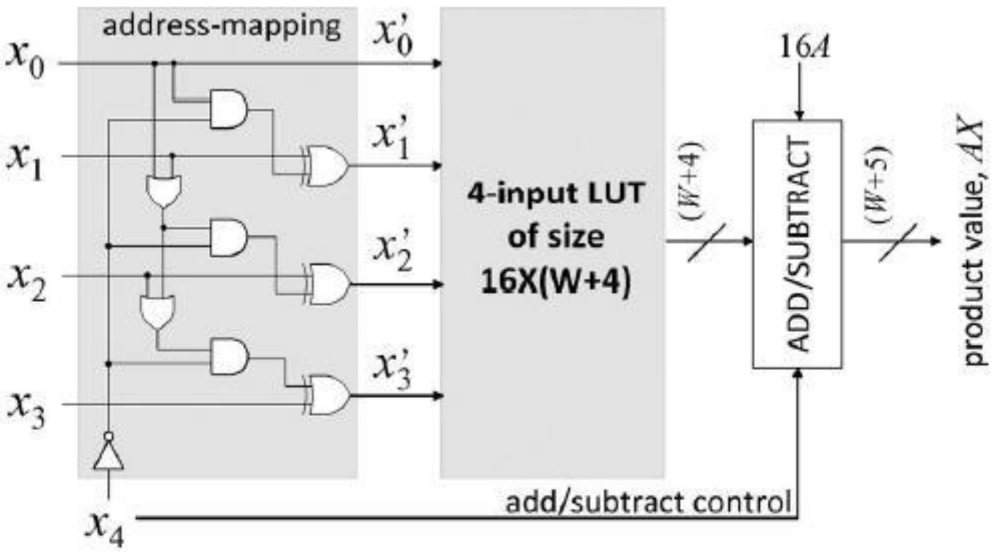


Fig 3. Optimized implementation of the sign modification of the odd LUT output.

1.4 LUT -BASED MULTIPLICATION USING APC - OMS MODIFIED OPTIMIZATION TECHNIQUE

The APC approach, although providing a reduction in LUT size by a factor of two, incorporates substantial overhead of area and time to perform the two's complement operation of LUT output for sign modification and that of the input operand for input mapping. However, we find that when the APC approach is combined with the OMS technique, the two's complement operations could be very much simplified since the input address and LUT output could always be transformed into odd integers.

1.5 LUT COMBINED APC-OMS BASED MULTIPLICAT-ION TECHNIQUE

input *X'* **12*^1 f>**	**product value**	***u*or shift***	**shifted input,** *X"*	**stored APC word**	**address** *dadzdido*
0 0 0 1	*A*	0	0 0 0 **1**	*PO = A*	0 00 0
0 0 10	*2 X A*	1			
0 10 0	*Ax A*	**9**			
10 0 0	8 x *A*	3			
0 0 **11**	*3A*	0	00 11	*PI = ZA*	0 00 1
0 1 1 0	*2* x 3.4	1			
1 1 0 0	4 x 3-4	2			
0 10 1	*5 A*	O	0 10 **1**	*P2* = 5i4	0 0 10
I 0 I 0	*2*x 5.4	1			
0 1 1 1	7*A*	0	0 1 1 1	*P3=7A*	0 0 11
1 1 1 0	2 x 7 *A*	1			
10 0 1	*QA*	0	1 0 0 **1**	*P4* = 9,4	0 10 0

10 11	*11A*	0	10 11	*P5 =11A*	0 10 **1**
1 1 0 **1**	13 A	Q	1 1 0 **1**	P6 = 13.4	0 1 1 0
1 1 1 1	*ISA*	0	1 1 1 1	P7 = 15.4	0 1 1 1

The proposed APC-OMS combined design of the LUT for L = 5 and for any coefficient width W is shown in Fig. 2.4. It consists of an LUT of nine words of (W + 4)-bit width, a four- to-nine-line address decoder, a barrel shifter, an address generation circuit, and a control circuit for generating the RESET signal and control word (s1s0) for the barrel shifter. The recomputed values of A x (2i + 1) are stored as Pi, for i = 0, 1, 2, . . . , 7, at the eight consecutive locations of the memory array, as specified in Table II, while 2A is stored for input X = (00000) at LUT address "1000," as specified in Table III. The decoder takes the 4-bit address from the address generator and generates nine word-select signals, i.e., {wi, for 0 < i < 8}, to select the referenced word from theLUT. The 4-to-9-line decoder is a simple modification of 3-to-8-line decoder.The control bits s0 and s1 to be used by the barrel shifter to produce the desired number of shifts of the LUT output are generated by the control circuit, according to the relations.

2. LUT OPTIMATION

2.1 Basic Components of LUT Optimization:

The modules contributed for combined APC-OMS based LUT optimization technique are

1 .Xin generation module (based on antisymmetric process)

2. Address generation module

3. line decoder 4. 9*(w+4) LUT >line selector module >multiplier result module >resultant multiplier module

5. Barrel Shifter

6. Add/Substractor (Sign Determination) module Xin generation module (based on antisymmetric process): A input of 5-bit length is given as input to this module. It used to generate antisymetric of last 4-bits (Xin(3 to 0)) when the msb of Xini.eXin(4) is ‗0‘ and and process the same input when the msb of Xin is ‗1‘ hence only 16 combinations will be achived for 5-bit of input as in table 1.

3. IMPLEMENTATION

A barrel shifter is often implemented as a cascade of parallel 2×1 multiplexers. For a 4-bit barrel shifter, an intermediate signal is used which shifts by two bits, or passes the same data, based on the value of S[1]. This signal is then shifted by another multiplexer, which is controlled by S[0]:

im = IN, if S[1] == 0 = IN << 2, if S[1] == 1

OUT = im, if S[0] == 0

= im<< 1, if S[0] == 1

It is used to add the intermediate results to 16A to get the final output .It may make output 0 when ‗clr‘ is high.

u = [(u + v)/2 − (v − u)/2] and

v = [(u + v)/2 + (v − u)/2], for (u + v) = 32A,

$$u = 16A - \left[\frac{v-u}{2}\right] \quad v = 16A + \left[\frac{v-u}{2}\right].$$

$$\text{Product word} = 16A + (\text{sign value}) \times (\text{APC word})$$

When xin(4) = ‗1‘ then sign value = 1

When xin(4) = ‗0‘ then sign value = 0.

4-bit_ripple_carry_adder-subtracter.svg In digital circuits, an adder-subtractor is a circuit that is capable of adding or subtracting numbers.This works because when D = 1 the A input to the adder is really A and the carry in is 1. Adding Bto a and 1 yields the desired subtraction of B - A.The adder-subtractor above could easily be extended to include more functions. For example, a 2-to-1 multiplexer could be introduced on each Bi that would switch between zero and Bi; this could be used (in conjunction_with D = 1) to yield the two's complement of A since —A = A + l.

clr
x
a
LUT
APC-OMS
output

Fig 4. 4-bit_ripple_carry_adder-subtracter

4. LUT APC - OMS Optimization Top Model output * LUT " APC-OMS

The APC approach, although providing a reduction in LUT size by a factor of two, incorporates substantial overhead of area and time to perform the two's complement operation of LUT output for sign modification and that of the input operand for input mapping.The proposed APC-OMS combined design of the LUT for L = 5 and for any coefficient width W is shown in Fig. 2.4. It consists of an LUT of nine words of (W + 4)-bit width, a four- to-nine-line address decoder, a barrel shifter, an address generation circuit, and a control circuit for generating the RESET signal and control word (s1s0) for the barrel shifter. The recomputed values of A x (2i + 1) are stored as Pi, for i = 0, 1, 2, . . . , 7, at the eight consecutive locations of the memory array, as specified in Table II, while 2A is stored for input X = (00000) at LUT address "1000," as specified in Table III. The decoder takes the 4-bit address from the address generator and generates nine word-select signals, i.e., {wi, for 0 < i < 8}, to select the referenced word from the LUT.

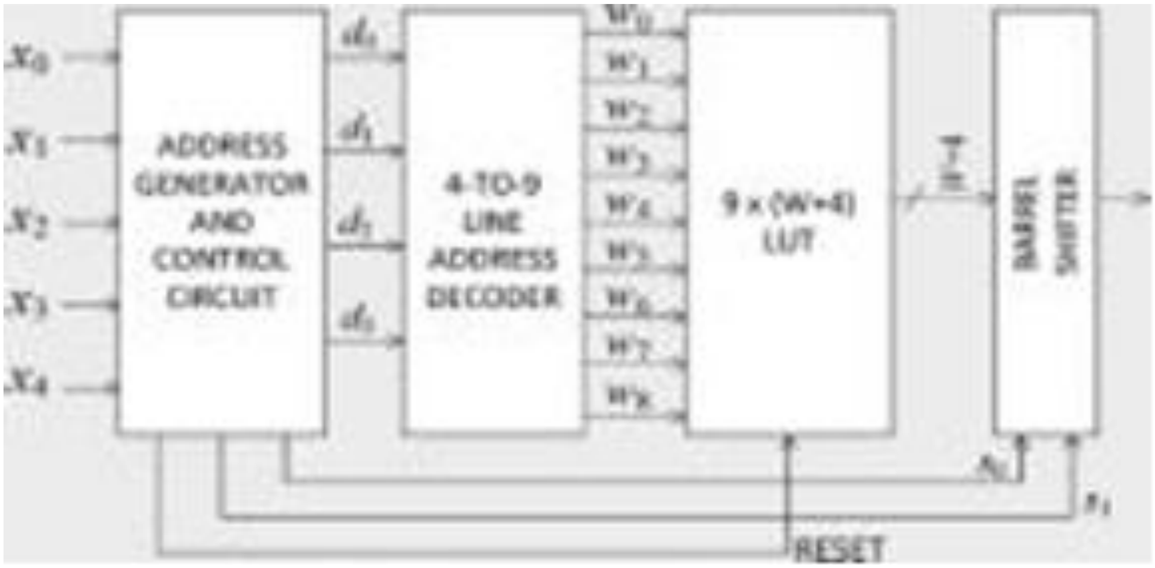
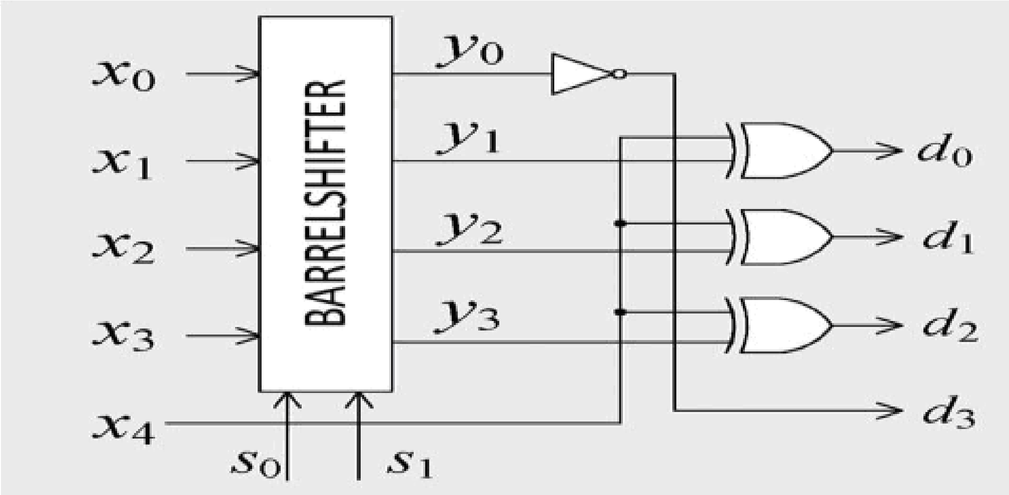


Fig 5 .4 lut combined apc-oms based multiplication technique



Here we observe that they will Antisymmetry in the address for the LSB 4 bits. We will get all the address from 0 to 15 for 0 to 31.Thus we reduce the memory locations required to store coefficients by half. Then we will store only odd coefficients in the look up table .Thus we reduce the number of coefficients by half again. On total we have reduced the number coefficients by quarter.

5. RTL SCHEMATIC:

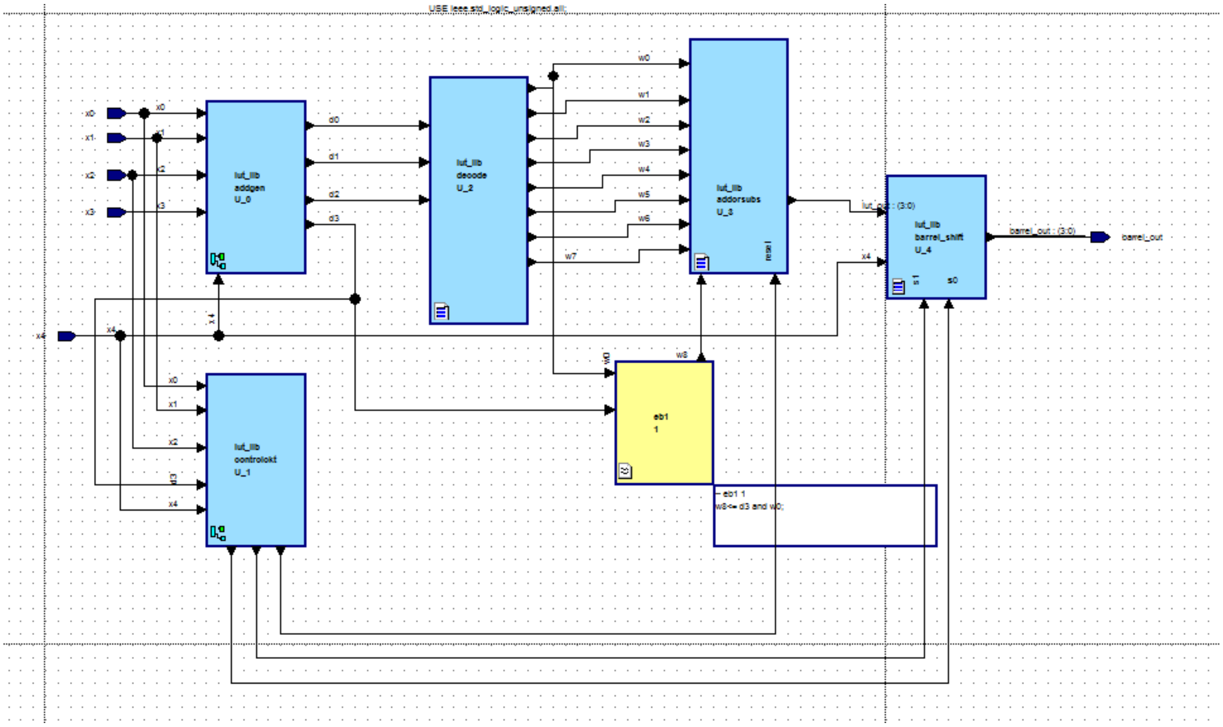


Fig 6. RTL Diagram

5. SIMULATION RESULTS:

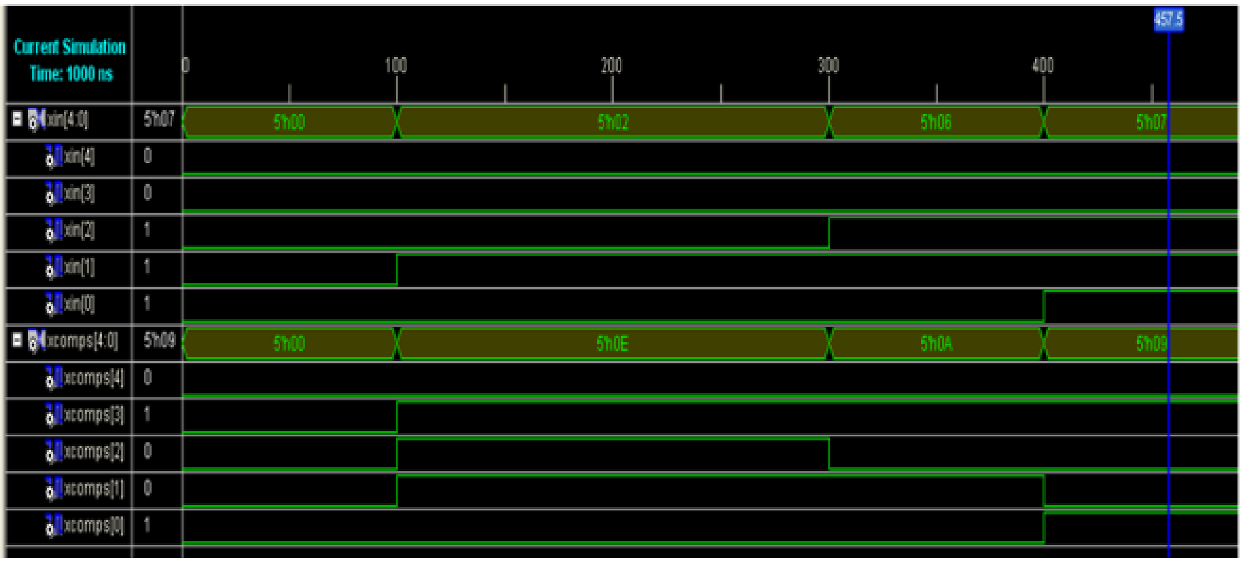


Fig. 7: Simulation Results of LUT of 6 bit

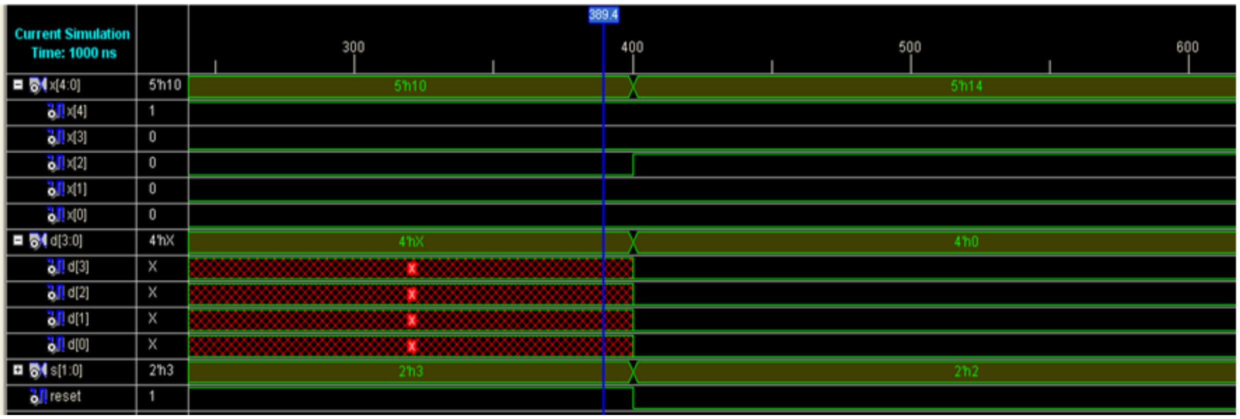


Fig 8.Simulation Results of LUT

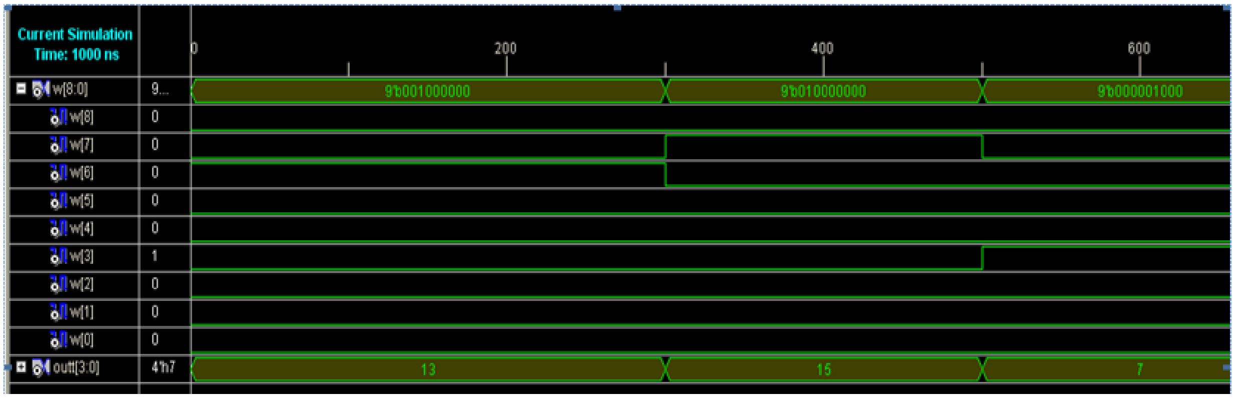


Fig 9. Simulation Results of LUT

6. CONCLUSION:

This paper deals with the design of the LUT prototype which can be applied to any DSP filter techniques or operations to reduce the LUT size over that of conventional design. By odd-multiple-storage scheme, for address-length 5, the LUT size is reduced to half, where is the word-length of the fixed multiplying coefficients. The proposed LUT-multiplier based design involves ¼ th of the memory than the conventional LUT-based design.

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